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REMOTELY PROGRAMMABLE ELECTRONIC TRIP SYSTEM

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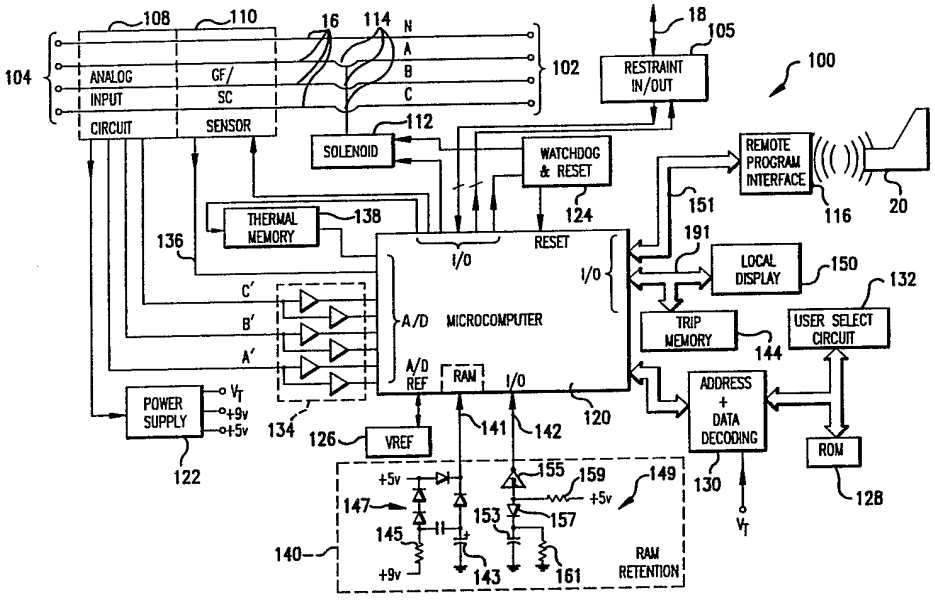

(57) Abstract

A remotely programmable breaker unit (100) for use in breaking current within a three phase current path (16) according to remotely programmable operating parameters is provided. Breaker unit (100) comprises a microcomputer (120) coupled between the current path and a trip solenoid (112) to programmably control trip parameter sent to and from a remote programmer (20). Breaker units are interconnected via a single zone selective interlocking (ZSI) line (18) to provide ZSI communication between the breaker units within an entire trip system (10). A method of remotely programming ground fault trip characteristics and short circuit trip characteristics in a trip system is also provided.

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REMOTELY PROGRAMMABLE ELECTRONIC TRIP SYSTEM

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to a method and apparatus for remotely programming multiple operating parameters into a breaker system. In particular, the method and apparatus of the present invention comprises one or more breaker units, each unit having remotely programmable trip characteristics.

Description of the Relevant Art

Trip systems used for breaking electrical flow to a load or current sink are well known in the art. Trip systems generally respond to current fluctuations in the power lines by activating a responsive open condition at the trip unit which detects the corresponding fluctuation. Most simple trip systems employ an electromagnet to trip the circuit in response to current or voltage fluctuations. The electromagnet provides a magnetic field in response to current flowing through the breaker unit. When the current level increases beyond a predetermined threshold, or trip point, the magnetic field "trips" a mechanism which causes a set of circuit breaker contacts to release, thereby "opening" or "breaking" the circuit path.

Many simple trip systems also employ a slower responding bi-metallic strip, which is useful for detecting subtle overload fault. This is because the extent of the strip's deflection represents an accurate thermal history of the circuit breaker and, therefore, even slight current overloads can be detected. Generally, the heat generated by the current overload will cause the bi-metallic strip to deflect into the tripping mechanism to open or break the circuit path.

The tripping systems described above have been useful for many years, but there has been an increasing demand for a more intelligent and precise tripping system. For example, many businesses today use expensive 3-phase power equipment which provides critical functions to the business and its customers. Due to the cost of the equipment and the functions that the equipment provide, the power supply to the equipment must be precisely measured and controlled. For this reason, microprocessor-based tripping systems have been developed in an attempt to provide programmable control to the equipment user.

A major problem in the design of microprocessor-based tripping systems has been the difficulty in programming the trip characteristics in each tripping unit. Quite often, a tripping system employs numerous trip or breaker units, and in order to reconfigure the system, each unit must be programmed at the unit cite. Thus, while microprocessor-based tripping systems can accurately and reliably measure the power provided to the equipment user, microprocessor-based tripping systems often require physical access and laborious programming of each unit. Each unit in the entire trip system must be separately programmed.

Three-phase power equipment is becoming more sophisticated requiring more flexibility in how the trip characteristics are configured. For example, equipment may be more sensitive to ground fault interrupt than to other forms of current fluctuation. Accordingly, the trip system must be quickly and easily reconfigured for ground fault interrupt in lieu of other forms of trip characteristics. Other equipment may be more sensitive to short circuit conditions, thereby requiring quick and easy reconfiguration for short circuit trip characteristics. Failure to quickly reconfigure each breaker or trip unit within a trip system to perform the specific designated trip function may result in inadvertent (nuisance) trips or missed trips which may damage the sophisticated three-phase power equipment attached at the current path load.

SUMMARY OF THE INVENTION

The problems outlined above are in large part solved by the apparatus and method of the present invention. While conventional microprocessor-based trip units require operator to physically contact the unit in order to reprogram trip characteristics, the trip system of the present invention comprises remote programmability to select units within the system. Thus, a trip system of the present invention can be quickly and easily reconfigured at a remote location. The engineer or operator need not physically contact each and every unit within the system in order to reconfigure the system trip characteristics to fit the specific need of the load power equipment. Remote programmability thereby can accommodate power equipment interchange by the trip characteristics necessary for a specific load.

Because each microprocessor-based trip unit is provided as a generic unit which can be programmed in the field to a desired characteristic, the present trip system is particularly suited for zone selective interlocking (ZSI) in which the location of a short circuit and/or ground fault is isolated and cleared without any harm to the load or any unintentional time delay. The present system provides a higher level of ZSI sophistication by allowing breaker units to communicate with each other over a single interconnect line and regardless of the type of current fluctuation (ground fault, overload, short circuit, etc.) encountered. Conventional microprocessor-based systems are generally limited to detection of only one specific current fluctuation (i.e., ground fault) and were generally incapable of reconfiguration to other forms of fluctuations. The microprocessor-based system of the present invention not only allows remote programmability but reconfiguration for various types of fluctuations as well as allowing remote power up or power down of one or more selective breaker units within the overall system. Accordingly, an important advantage of the present system is the ease by which the system can be reconfigured in a flexible format to receive and accommodate various trip points for substantially any form of current fluctuation.

Broadly speaking, the trip system of the present invention includes one or more programmable breaker units. Each programmable breaker unit comprises a 3-phase current path and a trip solenoid means for breaking the current path. A microcomputer is coupled between the current path and the trip solenoid having stored trip points which activate the trip solenoid when current within the current path exceeds the trip points. In addition, each breaker unit is remotely accessed via a remote programmer means which is coupled to the microcomputer for remotely monitoring the stored trip points. Each breaker unit may also include a trip system housing which contains the trip solenoid and microcomputer. The housing also includes a local display and binary coded decimal (BCD) input for allowing local programming of each unit if so desired.

In one preferred embodiment, the programmable trip system comprises at least one trip unit, or downstream trip unit, including three current sensors coupled to a 3-phase current path, and a microcomputer coupled to the sensors. The microcomputer is capable of adding AC current transmitted through all three

of the current sensors as well as measuring RMS current through each of the current sensors. A solenoid placed within the downstream trip unit can break the current path when the output of the added AC current and/or the output of the RMS current exceeds a plurality of stored trip points. The stored trip points are placed in a memory media within each microcomputer and can be remotely accessed and/or changed via a remote programmer. Accordingly, trip points for summed AC current (i.e., ground fault condition) or for RMS current (short circuit) can be remotely monitored and changed according to the specific type of load equipment used. Either ground fault of short circuit trip points can be remotely programmed into the system as well as the relative magnitudes of each trip point.

The present invention also contemplates a method for remotely programming ground fault trip characteristics and short circuit trip characteristics in a breaker system. This method comprises coupling at least two programmable breakers to a current path between the current path's source and load. The breakers are interconnected with a single interconnect line, and at least one breaker can be remotely programmed to break the current path when the current path receives current fluctuations which exceed a set of trip points stored within the respective breaker. Furthermore, a restraint out signal can be transmitted from the breaker to the other breaker over the single interconnect line. The restraint out signal is utilized for ZSI short circuit or ground fault isolation within the current path.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and advantages of the invention will become apparent upon reading the following detailed description and upon reference to the accompanying drawings in which:

FIG. 1a is a remotely programmable trip system according to the present invention;

FIG. 1b is a block diagram of a microprocessor based remotely programmable breaker unit of the present invention;

FIG. 2 is a perspective view of a remotely programmable breaker unit as set forth in the block diagram of FIG. 1b;

FIG. 3a is a diagram illustrating a local display 150 of FIG. 1b;

FIG 3b is a flow chart illustrating a manner in which a local processor 316 of FIG. 3a may be programmed to control an LCD display 322 of FIG. 3a;

FIG. 4 is a schematic diagram illustrating an analog input circuit 108, a sensor circuit 110, a gain circuit 134, and a power supply 122 of FIG. 1b;

FIG. 5 is a timing diagram illustrating the preferred manner in which signals received from the gain circuit 134 are sampled by the microcomputer 120 of FIG. 1b;

FIG. 6a is a side view of a rating plug 531 of FIG. 4;

FIG. 6b is a top view of the rating plug 531 of FIG. 4;

FIG. 7 is a schematic diagram illustrating a thermal memory 138 of FIG. 1b;

FIG. 8 is a schematic diagram illustrating the reset circuit 124 of FIG. 1b;

FIG. 9 is an illustration of a user select circuit 132 of FIG. 1b;

FIG. 10a is a diagram of the remote program interface 116 shown in FIG. 1b; and

FIG. 10b is a flow chart illustrating the configuration and programming protocol used in conjunction with the remote program interface 116 for down loading configuration parameters to the programmable trip system.

While the invention is susceptible to various modifications and alternative forms, a specific embodiment thereof has been shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that it is not intended to limit the invention to the particular form disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Turning now to the drawings, a remotely programmable tripping system 10 is illustrated in FIG. 1a. Tripping system 10 includes a power source 12 and a power load 14 connected by 3-phase current path or line 16. Line 16 carries phases A, B and C, as well as a neutral line, (N). Tripping system 10 also includes one or more remotely programmable breaker units 100 coupled to current path 16. Each unit 100 is interconnected with a single ZSI conductor 18. ZSI line 18 allows units 100 to communicate with each other in a zone selective interlocking configuration. ZSI, and its mode of operation, will be described in detail below.

Along with ZSI interface and communication capabilities, the present invention also provides remote programmability of selective units 100 via remote programmer 20.

The present invention has direct application for monitoring and interrupting a current path in an electrical distribution system according to parameters which may be programmed by the user at a remote location via programmer 20. Furthermore, the user can monitor current flowing within path 16 at remote programmer 20. Thus, programmer 20 either transmits or receives optical configuration signals 22 which correspond with the internal configuration or set point configuration of each unit 100. Also, signals 22 include current and/or voltage readings taken from line 16 as well as trip history maintained within each unit 100. It is important to note that any form of current or trip indicia can be sent via signals 22 and analyzed, acted upon or monitored by programmer 20. As will be discussed below, the various indicia, of which can be accessed by programmer 20, is useful in reconfiguring and monitoring the entire system 20 based upon any changes made to either source 12 or load 14. Accordingly, the present invention allows a generic unit 100 be placed in the field and programmed at a remote location to any form of trip format or desired operating parameters dictated by the end user. The generic unit 100 thereby achieves advances over previous computer or microprocessor-based systems. In addition, ZSI line 18 allows direct interface between units 100 to provide restraint in/out isolation of either short circuit or ground fault conditions without using multiple ZSI lines.

FIG. 1b shows a block diagram of programmable breaker unit 100 for use with 3-phase current path 16 having source inputs 102 and load outputs 104. Breaker unit 100 uses an analog input circuit 108 and a GF/SC sensor 110 to detect 3-phase current on the current path 16. When the tripping system detects any form of current fluctuation such as short circuit, ground fault, overload, or otherwise determines that the current path should be interrupted, it engages a solenoid 112 which trips a set of contactors 114 to break the current path carrying phases A, B and C. Consequently, any current fluctuations such as short circuit or ground fault circuit through the earth ground path or through an optional neutral line (N) may be broken.

Breaker unit 100 utilizes a number of circuits to determine when current path 16 should be interrupted. This determination is centralized at a microcomputer 120, preferably an MC68HC11A1, which is described in MC68HC11 HCMOS Single Chip Microcomputer Programmer's Reference Manual, 1985 and MC68HC11A8 Advanced Information HC Single Chip Microcomputer, 1985, all being available from Motorola, Inc., Schaumburg, Illinois. Peripheral circuits that support microcomputer 120 include a reset circuit 124 that verifies the sanity of breaker unit 100, a voltage reference circuit 126 that provides a stable and reliable reference for analog to digital (A/D) circuitry located within the microcomputer 120, ROM 128 that stores the operating instructions for the microcomputer 120, and a conventional address and data decoding circuit 130 for interfacing the microcomputer 120 with various circuits including the ROM 128 and a user select circuit 132. The address and data decoding circuit 130, for example, includes an address decoder part No. 74HC138 and an eight-bit latch, part No. 74HC373, to latch the lower eight address bits which are alternatively multiplexed with eight data bits in conventional fashion. The ROM, for example, is part No. 27C64. The user select circuit 132 allows the user to physically contact the outer face of breaker unit 100 and to programmably designate tripping characteristics for breaker 100, such as short circuit, overload and phase imbalance fault (ground fault) conditions. Thus, not only may unit 100 be remotely programmed, but user select circuit 132 provides that, as a backup, each unit 100 can be locally programmed on the outer face of the unit.

Breaker unit 100 is operatively coupled with a conventional electrical distribution system through a restrain in/out circuit 105. As shown in FIG. 1a, signals received over ZSI line 18 from a "downstream" breaker unit 100 indicate that a current fluctuation condition is present between the downstream unit 100 and load 14. Thus, the downstream unit 100 transmits, via ZSI line 18, a restraint signal to the upstream unit 100 to signal a delay or restraint on the upstream unit to allow the downstream unit a chance to trip first. Thus, ZSI allows coordination between the units so that when a downstream breaker senses a current fluctuation, it sends a restraint signal to the upstream breaker instructing that breaker to carry out a selected or programmable time delay. If the upstream circuit breaker does not receive a restraint signal from a downstream breaker, it ignores the remotely programmed trip delay setting and trips instantaneously. Thus, the trip unit shown in FIG. 1b can either receive restraint information from a downstream or it can transmit restraint information to an upstream unit via restraint in/out circuit 105 and ZSI line 18. Unit 100 uses these restraint signals in conjunction with its ground fault and short circuit protection functions.

Ground faults are a result of leakage current to earth in an electrical distribution system. The leakage current level is usually low compared to the normal loading characteristics of an electrical circuit or load 14. Protection levels for ground fault on an industrial circuit breaker unit would typically be adjustable from 20% to 75% of the circuit breaker unit's full load current carrying capacity. The ground fault trip delay is adjustable from 0.1 to 0.5 seconds. If a circuit breaker unit 100 detects a ground fault it will immediately raise its restraint-out line 105 to communicate, via ZSI line 18, to an upstream breaker unit that a fault condition has been detected. This upstream breaker unit is then said to be "restrained". Any breaker witnessing a ground fault must receive a ground fault restraint signal from a downstream breaker within 33 milliseconds or it will initiate an immediate trip without delay. If it receives a restraint signal from a downstream breaker, it will begin its time delay and trip after time-out unless the fault is removed from the downstream breaker unit. Because ground fault protection is not required for all circuits, it may or may not be installed depending upon the type of load 14 or tripping system 10 desired.

Short circuits are similar in nature to ground faults with the exception that the fault current is not generally leakage to earth but rather a high current short to a normal circuit conductor. Short circuit protection levels are typically adjustable from 200% to 1000% of the breaker unit's full load carrying capacity. The short circuit trip delay time is adjustable, for example from 0.1 to 0.5 seconds. Time delay short circuit protection is not required for all circuits and may or may not be installed.

Because of the obvious difference in fault level, it should be apparent that ground fault restraint signals must be differentiated from short circuit restraint signals. Typically two sets of restraints have been used in conventional units which would provide the independent fault restraining signals required for both ground fault and short circuit functions. Thus, conventional tripping systems which require ground fault and short circuit protection utilize at least two ZSI lines 18. Conversely, the present invention requires only one ZSI line 18 since each unit 100 can be reconfigured for short circuit, ground fault, or short circuit and ground fault, the conditions of either being transmitted over a single ZSI line to interconnected units 100. The geographic location between upstream and downstream breaker units may be much as 1000 feet, making installation and maintenance of numerous communication links, or ZSI lines 18, quite expensive. In addition, the electronic circuitry and connection means for restraint signals becomes difficult and costly on small frame circuit breaker units. If duplicative ground fault and short circuit restraint in/out circuits are required, then breaker unit space is needlessly wasted in conventional units. Conversely, the present invention utilizes only one restraint in/out circuit 105, useable for ground fault and/or short circuit, wherein all ZSI communication is achievable over a single interface ZSI line 18.

Breaker unit 100 requires circuitry for only one restraint in/out circuit 105 with the restraining function, either ground fault or short circuit, performed via an option in the configuration programming protocol. Remote programmer 20 communicates over transmission media, optical configuration signals 22 to a local remote program interface 116 electrically coupled to microcomputer 120 as shown in Figure 1b. Programmer 20 thus monitors microcomputer 120 at a remote

location to set ZSI configuration bits in the resident non-volatile memory of the microcomputer 120. These bits indicate the type of ZSI response that the trip system is to perform with respect to a given fault condition. If the ground fault ZSI bit is set to logic 1, the breaker unit 100 will treat the restraint in/out circuit 105 with reference to ground fault protection. If the short circuit ZSI bit is set to logic 1, the breaker unit 100 will treat the restraint in/out circuit 105 with reference to short circuit protection. If both ground fault ZSI bit and short circuit ZSI bit are set to logic 1, breaker unit 100 will respond according to the fault condition it detects. In this case, should ground fault and short circuit fault be detected simultaneously, breaker unit 100 will preform independent time delays and trip contactors 114 when the shortest time delay expires. In the case where ZSI bit is a logic 0, breaker unit 100 will always perform a delayed trip function on that fault condition.

The selectable ZSI approach provides a flexible and less expensive alternative to the conventional independent and duplicative restraint circuits incurred prior to the present invention. For further details regarding restraint in/restraint out electrical distributions systems of conventional design, reference may be made to U.S. Patent No. 4,706,155 to Durivage *et al.*

Other circuits are used along with the above circuits to provide reliability and integrity to the breaker unit 100. For instance, the microcomputer 120 utilizes the analog input circuit 108 along with a gain circuit 134 to measure precisely the RMS (Root Mean Squared) current on each phase of the lines 16. The accuracy of this measurement is maintained even in the presence of non-linear loads.

The analog input circuit 108 develops phase signals A', B' and C' that are representative of the current on lines 16. The gain circuit 134 amplifies each phase signal A', B' and C' through respective dual gain sections, from which the microcomputer 120 measures each amplified signal using its A/D circuitry. By providing two gain stages for each signal A', B' and C', the microcomputer 120 can immediately perform a high gain or low gain measurement for each current phase depending on the resolution needed at any given time.

The analog input circuit 108 is also utilized to provide a reliable power source to the breaker unit 100. Using current developed from the lines 16, the analog input circuit 108 operates with a power supply 122 to provide three power signals (VT, +9v and +5v) to breaker unit 100. The power signal VT is monitored by the microcomputer 120 through decoding circuit 130 to enhance system dependability.

System dependability is further enhanced through the use of a thermal memory 138 which the microcomputer 120 interacts with to simulate a bi-metal deflection mechanism. The thermal memory 138 provides an accurate secondary estimate of the heat in the breaker unit 100 in the event power to the microcomputer 120 is interrupted.

GF/SC sensor 110 is used to detect the presence of any form of GF/SC current or voltage fluctuations (e.g., overload, ground faults and/or short circuits) on one or more of lines 16, and to report the faults via input line 136 to the microcomputer 120. Using user selected trip characteristics, the microcomputer 120 determines whether or not the fluctuations are present for a sufficient time period at a sufficient level to trip the contactors 114. The microcomputer 120 accumulates the ground fault and/or short circuit delay time in its internal RAM. A RAM retention circuit 140 is used to preserve the ground fault history for a certain period of time during power interruptions.

The RAM retention circuit 140 exploits the built-in capability of the microcomputer 120 to hold the contents of its internal RAM provided that an external supply voltage is applied to its MOPDB/Vstby input 141. This external supply voltage is stored on a 150 microfarad electrolytic capacitor 143 that is charged from the +9 volt supply through a 6.2 K ohm resistor 145. The capacitor 143 is charged from the +9 volt supply, and clamped by diodes to the +5 volt supply, so that the capacitor will be rapidly charged during power-up.

The ground fault and/or short circuit delay time stored in internal RAM becomes insignificant after a power interruption that lasts longer than about 3.6 seconds. To test whether such an interruption has occurred, the RAM retention circuit 140 includes an analog timer 149 having a resistor 161 and a capacitor 153 establishing a certain time constant, and a Schmitt trigger inverter 155 that senses

whether the supply of power to the microcomputer 120 has been interrupted for a time sufficient for the capacitor 153 to discharge. Shortly after the microcomputer reads the Schmitt trigger 155 during power-up, the capacitor 153 becomes recharged through a diode 157 and a pull-up resistor 159. Preferred component values, for example, are 365 Kohms for resistor 161, 10 microfarads for capacitor 153, part No. 74HC14 for Schmitt trigger 155, 1N4148 for diode 157, and 47 Kohms for resistor 159.

Another important aspect of breaker unit 100 is its ability to transfer information between itself and the remote or local user. This information includes the real-time current and phase measurements on lines 16, the system configuration or trip points stored within breaker unit 100 and information relating to the history of trip causes (reasons why the microcomputer 120 tripped the contactors 114). As discussed above, the real-time line measurements are precisely determined using the analog input circuitry 108 and the gain circuit 134. The system configuration of breaker unit 100 and other related information is readily available from ROM 128 and the user select circuit 132. The information relating to the history of trip causes is available from a nonvolatile trip memory 144. Information of this type is displayed for the user either locally at a local display 150 or remotely at a conventional display terminal of remote programmer 20 via remote program 116.

To communicate with the remote program interface 116, the tripping system utilizes a serial communication interface 151 functionally derived by the asynchronous communication interface internal to the microcomputer 120. Preferably, using the MC68HC11, the serial communication interface (SCI) can be achieved internal to microcomputer 120.

Breaker unit 100 configuration parameters can be downloaded into the nonvolatile memory (EEPROM) resident within the microcomputer 120 from remote programmer 20 via program interface 116. Specifically, the circuit breaker type, current carrying capacity and zone selective interlocking functions are configured by this program interface 116. The data may be stored in the nonvolatile memory resident using multiple (adjacent) cells to check for data corruption. The data bytes are stored in even cell addresses with their 2's

complement stored in the next odd cell. If the sum of the data byte pair (data and 2's complement) does not equal zero, then that data is corrupt. The data is stored at 2 location pairs in the EEPROM (separated by at least 1 page), and the data is verified in both location pairs. If any of the pairs do not correspond with the other, or do not sum to zero individually, the data is corrupt and the pair that sums to zero is assumed to be correct. This value is rewritten to the next pair of cells. The cell set that was corrupted is rewritten such that the cell pairs sum to OFFH implying bad cells. Before any data can be rewritten, all data is read and safely stored for security.

For example, all data is read from the EEPROM into temporary RAM, using a combination of configuration byte counter and end of data marker. This assures that all configuration data is safely stored to RAM and the EEPROM data is correctly copied. After all configuration data has been read, both the original and redundant data pairs are checked for validity. If any data is found to be bad, the remaining data is shifted (opening two memory locations after the bad data), the data is reconstructed from the remaining good pair and the data is stored at the opened locations. The bad data cells are then marked with OFFH, and a bad EEPROM cell flag is set. After all configuration data has been checked, and corrected if necessary, it is copied to RAM. If the bad EEPROM cell flag is set, the corrected data is rewritten from temporary RAM into the EEPROM.

Accordingly, trip points are stored in a redundant form in nonvolatile, remotely-programmable memory such that upon an inadvertant loss of trip point data therein, the microcomputer recovers an error-free copy of the data.

Fig. 10a is a circuit diagram illustrating program interface 116. In general, program interface 116 provides a means of electrically isolating the communication signals between the remote programmer 20 and the tripping system's serial communication interface 151. The electrical isolation is achieved through the use of optocouplers 781 and 782 shown in Fig. 10a; otherwise, the program interface connection is preferably an electrical connection (although other forms, e.g., radio communication, may be used). The resistors 783 and 784 limit the current flowing in a respective receive circuit 777 and transmit circuit 778 respectively. The transmit drive transistor 785 provides current drive for the transmit circuit

778. Schmitt trigger 786 provides a data inversion for the transmit drive transistor 785. Another Schmitt trigger 787 provides data inversion and squaring of the digital data edges coming from the receiver optocoupler 781.

Preferred components for the program interface 116 are 1.0 Kohm for resistor 783, 270 ohm for resistor 784, part No. 4n35 for the optocouplers 781 and 782, part No. BS170 for the drive transistor 785 and part No. 74hc14 for the Schmitt triggers 786 and 787.

FIG. 2 is a perspective view of the tripping system 100 as utilized in a circuit breaker housing or frame 210. The lines 16 carrying phase currents A, B and C are shown passing through line embedded current transformers 510, 512 and 514 (in dashed lines) which are part of the analog input circuit 108. Once the solenoid 112 (also in dashed lines) breaks the current path in lines 106, the user reconnects the current path using a circuit breaker handle 220.

Except for the circuit breaker handle 220, the interface between the breaker unit 100 and the user is included at a switch panel 222, an LCD display panel 300 and a communication port 224. The switch panel 222 provides access holes 230 to permit the user to adjust binary coded decimal (BCD) dials (FIG. 8) in the user select circuit 132. The communication port 224 is used to receive or transmit information as described above to the remote programmer 20 via an optic transmission channel. Thus, set point data may be entered either locally via holes 230 or remotely via communication port 224.

In the following sections, the breaker unit 100 is further described in detail.

A. Local Display

FIG. 3a is a schematic diagram of the local display 150 of FIG. 1b. The local display 150 is physically separated from the remaining portion of the breaker unit 100, but coupled thereto using a conventional connector assembly 310. The connector assembly 310 carries a plurality of communication lines 312 from the microcomputer 120 to the local display 150. These lines 312 include tripping system ground, the +5V signal from the power supply 122, serial communication lines 314 for a display processor 316, and data lines 318 for a latch 320. The data lines 318 include four trip indication lines (overload, short circuit, ground fault

and phase unbalance) which are clocked into the latch 320 by yet another one of the lines 318.

An LCD display 322 displays status information provided by the latch 320 and the display processor 316. Different segments of the LCD display 322 may be implemented using a variety of devices including a combination static drive/multiplex custom or semi-custom LCD available from Hamlin, Inc., Lake Mills, Wisconsin. For additional information on custom or semi-custom displays, reference may be made to a brochure available from Hamlin, Inc. and entitled Liquid Crystal Display.

The latch 320 controls the segments 370-373 to respectively indicate the trip conditions listed above. Each of these segments 370-373 is controlled by the latch 320 using an LCD driver circuit 326 and an oscillator circuit 328. The corresponding segment 370-373 illuminates when the associated output signal from the latch 320 is at a logic high level.

The display processor 316 controls four seven-segment digits 317 as an ammeter to display the current in the lines 16. The display processor 316, for example, is an NEC part No. UPD7502 LCD Controller/Driver which includes a four-bit CMOS microprocessor and a 2k ROM. This NEC part is described in NEC UPD7501/02/03 CMOS 4-Bit Single Chip Microprocessor User's Manual, available from NEC, Mountain View, Ca. Other segments 375 of the LCD display 322 may be controlled by the display processor 316 or by other means to display various types of status messages.

For example, a push button switch 311 may be utilized to test a battery 338. To perform this test, the battery 338 is connected through a diode 313 to one of the segments 375 so that when the switch 311 is pressed, the condition of the battery is indicated. The push-button switch 311 preferably resets the latch 320 when the switch is depressed. For this purpose the switch 311 activates a transistor 315. The latch, for example, is a 40174 integrated circuit.

Additionally, the switch 311 may be used to select the phase current to be displayed on the LCD display 322 to control segments 375 such that they identify the phase current (A, B, C or N) on lines 16 being displayed on the four seven-segment digits 317. For this purpose the switch 311 activates a transistor 327 to

invert a signal provided from the battery and to interrupt the display processor 316. Each time the display processor 316 is interrupted, the phase current that is displayed changes, for example, from phase A to B to C to ground fault to A, etc.

An optional bar segment 324 is included in the LCD display 322 to indicate a percentage of the maximum allowable continuous current in the current path. The bar segment 324 is controlled by the +5V signal via a separate LCD driver 330. The LCD driver 330 operates in conjunction with the oscillator circuit 328 in the same manner as the LCD driver 326. However, the LCD driver 330 and the oscillator circuit 328 will function at a relatively low operating voltage, approximately two to three volts. An MC14070 integrated circuit, available from Motorola, Inc., may used to implement the LCD drivers 330 and 326. Thus, when the tripping system fails to provide the display processor 316 with sufficient operating power (or current), the LCD driver 330 is still able to drive the bar segment 324. The LCD driver 330 drives the bar segment 324 whenever the tripping system detects that less than about 20% of the rated trip current is being carried on lines 16 to the load 14.

As an alternative embodiment, the bar segment 324 may be disabled by disconnecting the LCD driver 330.

Additional bar segments 332-335 are driven by the display processor 316 to respectively indicate when at least 20-40%, 40-60%, 60-80% and 80-100% of the rated trip current is being carried on lines 106 to the load.

The oscillator 328 also uses part No. MC14070 in a standard CMOS oscillator circuit including resistors 329, 336 and a capacitor 331 that have values, for example, of 1 megohm, 1 megohm, and 0.001 microfarads, respectively. Even when a power fault causes the system to trip and interrupt the current on lines 16, the local display 150 is still able to operate on a limited basis. This sustained operation is performed using the battery 338 as a secondary power source. The battery, for example, is a 3 to 3.6 volt lithium battery having a projected seventeen year life. The battery 338 supplies power to portions of the local display 150 only when two conditions are present: (1) the latch 320 has received a trip signal from the microcomputer 120 (or the test switch 311 is activated), and (2) the output voltage level of the +5V power supply is less than

the voltage level from the battery 338. When the latch 320 latches in any one of the four trip indication lines from the data lines 318, a control signal is generated on a latch output line 340. The control signal turns on an electronic switch 342 which allows the battery 338 to provide power at Vcc so long as a diode 344 is forward biased.

The diode 344 is forward biased whenever the second condition is also present. Thus, when the output voltage level of the +5V power supply is less than the voltage level from the battery 338, the diode 344 is forward biased and the battery 338 provides power to the local display 150. In addition, the diode 344 is forward biased until a switch 346, activated by a power-up circuit 348, allows the +5V signal to provide power at Vcc. The power-up circuit 348 activates the electronic switch 346 only after resetting the display processor 316. The power-up circuit 348, for example, is part No. ICL7665 working in connection with resistors 349, 351, and 353 having values of 620 Kohms, 300 Kohms and 10 megohms, respectively.

Power is provided from Vcc only to the latch 320, the LCD driver 326, the LCD driver 330, and the oscillator circuit 328. The LCD driver 330 and the oscillator circuit 328 receive power from either the battery 338 or the +5V power supply output via diodes 350 and 352. This arrangement minimizes current drain from the battery 338 while allowing the user to view the status of the tripping system 100 during any power fault situation.

Power cannot be drawn from the battery 338 unless the battery 338 is interconnected with the remaining portion of the tripping system via connector 310, because the connector 310 provides the ground connection for the negative terminal of the battery 338. This aspect of the local display 150 further prolongs battery life and therefore minimizes system maintenance.

In FIG. 3b, a flow chart illustrates the preferred programming of the display processor 316. The flow chart begins at block 376 where the memory internal to the display processor is initialized. The memory initialization includes clearing internal RAM, input\output ports and interrupt and stack registers.

At block 378, a software timer is reset and the display processor waits for a data ready flag which indicates that data has been received from the

microcomputer 120 of FIG. 1b. The software timer provides a conventional software watchdog function to maintain the sanity of the display processor. If the software timer is not reset periodically (within a certain time interval), the display processor resets itself.

The data ready flag is set in an interrupt routine, illustrated by blocks 390 through 398 of FIG. 3b. The display processor is programmed to execute the interrupt routine when it receives data from the microcomputer 120 of FIG. 1b. At block 390 of the interrupt routine, a test is performed to determine whether the data byte just received is the last data byte of the packet sent from the microcomputer. If the data byte just received is not the last data byte, flow proceeds to block 398 where a return-from-interrupt instruction is executed. If the data byte just received is the last data byte, flow proceeds to block 392.

At block 392, a test is performed to determine the integrity of the received data packet. This is accomplished by comparing the 8-bit sum of the previously received 7 bytes with the most recently received byte (last byte). If the 8-bit sum and the last byte are different, flow proceeds to block 398. If the 8-bit sum and the last byte are the same, the display processor sets the data ready flag, depicted at block 396, and returns from the interrupt, via block 398, to block 380. At block 380, the received data is stored in memory and the data ready flag is reset.

At blocks 382 and 384, the display processor utilizes a conventional conversion technique to convert the stored data to BCD format for display at the LCD display 322 of FIG. 3a. The data that is sent and displayed at the LCD display 322 is chosen by the operator using the switch 311 to sequence through each of the three phase currents and the ground fault current, as indicated in the data that is received from the microcomputer 120.

At block 386, the display processor utilizes received data, including the sensor identification, the rating plug type and the long-time pickup level, to determine the percentage of rated trip current (short circuit or ground fault) being carried on lines 16. At block 388, the bar segments (324 and 332-335 of FIG. 3a) are driven by the display processor in response to this determination. From block 388, flow returns to block 378.

Blocks 400-406 of FIG. 3b represent a second interrupt routine that the display processor may be programmed to execute in response to the depression of the switch 311. At block 400 of this second interrupt routine, the display processor determines which phase (short circuit or ground fault) current the operator has selected by depressing the switch 311. At blocks 402 and 404, the display processor monitors its I/O port to determine when the switch 311 is released and to debounce the signal received from the switch 311. At block 406, the display processor executes a return from interrupt command.

It should be noted that the display processor 316 is optional for the local display 150 and therefore not required for its operation. Further, the local display 150 is itself an option to the tripping system and is not required for operating the tripping system.

B. Short Circuit Current and Ground Fault Detection

FIG. 4 illustrates an expanded view of the analog input circuit 108, SC/GF sensor 110, power supply 122 and the gain circuit 134 of FIG. 1b. Each of these circuits receive power from the three-phase current lines 16. Using this power, these circuits provide signals from which breaker unit 100: (1) determines the phase and current levels on lines 106 and detects the presence of a short circuit, (2) detects the presence of a ground fault and instantaneous short circuits, (3) provides system power, and (4) establishes its current rating.

(1) Determining Phase And Current Levels And Detecting Short Circuits

In FIG. 4, the analog input and GF/SC sensing circuits 108 and 110 include current transformers 510, 512 and 514 that are suitably located adjacent the lines 16 for receiving energy from each respective phase current path A, B, and C. Each current transformer 510, 512 and 514 is constructed to produce a current output that is proportional to the primary current in a fixed ratio. This ratio is set so that when the primary current is 100% of the rated current

transformer size (or sensor size), the current transformer is producing a fixed output current level. For example, for a 200 amp circuit breaker, each current transformer 510, 512 and 514 will produce the same current output signal when operating at 100% (200 amps) as a current transformer in a 4000 amp circuit breaker which it is operating at 100% (4000 amps). The preferred construction yields a current transformer output current of 282.8 milliamps (RMS) when the primary current is 100% of the rated current.

The output currents provided by the transformers 510, 512 and 514 are routed through a ground fault sensing toroid 508, full wave rectifier bridges 516, 518 and 520 and the power supply 122 to tripping system ground. The output currents are returned from tripping system ground through a burden resistor arrangement 530. Sensing toroid 508 sums the output currents from the transformers 510, 512 and 514. In a system utilizing a neutral (N) line 16, sensing toroid also sums the output current from a transformer 506, which is coupled to the neutral line (N) to sense any return current. A signal representing this current summation is produced at an output winding 509 and is carried to a fourth rectifier bridge 522, which is used to detect short circuit or ground fault conditions.

On the right (positive) side of the rectifier bridges 516-522, positive phase current signals are produced and added together at lead 524. The current at lead 524 is used for the power supply 122, which is discussed in a later part of this section.

On the left (negative) side of the rectifier bridges 516-520, negative phase current signals are carried through the burden resistor arrangement 530 and

tripping system ground, and are returned to the rectifier bridges 516-520 through the power supply 122. This current path establishes voltage signals A', B' and C', each referred to as a burden voltage, for measurement by the microcomputer 120 via the gain circuit 134.

In FIG. 4, the signals A', B' and C' are presented to the respective dual gain sections for inversion and amplification. The gain circuit 134 of FIG. 4 is shown with one of its three identical dual gain sections, generally designated as 533, in expanded form. The dual gain section 533 receives phase signal A'. Each dual gain section includes a pair of low pass filters 532 and a pair of amplifiers 534 and 536. The low pass filters 532 provide noise suppression, and the amplifiers 534 and 536 reduce the signal magnitude by 0.5 and increase the signal magnitude by a factor of 3, respectively, for the desired resolution. This arrangement allows the microcomputer 120 to instantaneously measure these current levels without changing any gain circuitry. Preferred component values are, for example, 10 Kohms for resistors 541, 543, 545, 553 and 555; 4.75 Kohms for resistors 547 and 559; 60 Kohms for resistor 557; and 0.03 microfarads for capacitors 549 and 561. The amplifiers 551 and 663 are, for example, part No. LM124.

Using the gain circuit 134, the microcomputer 120 measures the true RMS current levels on lines 106 by sampling the burden voltages developed at signals A', B' and C'. The RMS calculations are based on the formula:

$$I_{RMS}^2 = \sum_{t=0}^{N} I(t)^2$$

where:

N	=	the number of samples;
t	=	time at discrete intervals (determined by sample rate); and
I(t)	=	the instantaneous value of the current flowing through the breaker.

The current flowing through the circuit breaker is sampled at fixed time intervals, thereby developing I(t). The value of this instantaneous current sample is squared and summed with other squared samples for a fixed number of samples N. The mean of this summation is found by dividing it by N. The final RMS current value is then found by taking the square root of the mean.

In FIG. 5, an example of a rectified sinusoidal current waveform is illustrated for 1.5 cycles of a 60 hertz signal with a peak amplitude of 100 amps. The sampled current is full wave rectified. The vertical lines represent the discrete points in time that a current value is sampled. With a sample rate of 0.5 milliseconds, over 25 milliseconds of time, 50 samples will be taken.

The other columns in TABLE 1 detail the binary equivalent data that the microcomputer would process using the ratio that 100 amps equals 255 binary.

The value I_{RMS} will accurately reflect the heating effect of the current waveform that existed from t = 0 to t = N. This current waveform is typically an A.C. waveform with a fundamental frequency of 50 to 60 Hertz, but may contain many upper harmonics (i.e., multiples of the fundamental frequency).

In practical implementations, several factors affect the accuracy of the I_{RMS} calculation, including the sample rate and the number of samples. In the preferred embodiment, the sample rate is 2,000 Hertz and at least 128 samples are taken before the current magnitude is estimated.

Accordingly, by regularly measuring the RMS current levels numerous calculations may be made, and RMS short circuit threshold levels may be detected.

(2) Detecting The Presence Of A Ground Fault And Instantaneous Short Circuit Levels

The sensing toroid 508 magnetically adds the current signals from the input windings 540, 542, 544 and 546 to indicate whether a ground fault or an instantaneous short circuit is present on lines 106. The toroid 508 is constructed with four identical input windings 540, 542, 544 and 546; one for each of the current transformers 510, 512 and 514 and one for the neutral current path transformer 506, which is optional. The toroid 508 has a single output winding 509 which provides a summed current signal.

The ground fault sensing toroid 508 includes another winding 550 to allow a test signal to be applied at terminals 552. Using momentary switch 554, the test signal creates a pseudo ground fault for the tripping system. The tripping system reacts to this pseudo ground fault in the same manner as a true ground fault. The test winding 550 is protected by a positive coefficient resistor 556 that increases its resistance as it heats, thereby limiting the current through it and the winding 550. The positive coefficient resistor is, for example, a Keystone PTC Resettable Fuse, part No. RL3510-110-120-PTF. The test winding 550 eliminates the need for a separate test transformer, which has been utilized by systems in the prior art.

The operation of sensing toroid 508 is best understood by considering the operation of the tripping system with a ground fault and without a ground fault. In a balanced three phase system without a ground fault, the current magnitude in each phase is equal but 120 degrees out of phase with the other phases, and no

neutral current exists; thus, the output winding 509 produces no current. As the current through any phase (A, B or C) increases, the current in the neutral path is vectorially equal in magnitude but opposite in direction to the increase in phase current, and the magnetic summation is still zero. When a ground fault is present, current flows through an inadvertent path to an earth-grounded object, bypassing the neutral transformer 506 and creating a current signal in the transformer 509. Thus, the transformer 509 produces a current signal only when a ground fault is present.

The current signal from the output transformer 509 of the ground fault sensing toroid 508 is routed through the rectifier bridge 522, the power supply 122 and returned through the burden resistor arrangement 530. In conjunction with the rectifier bridge 522, the burden resistor arrangement 530 converts that current signal into an A.C. rectified signal 558 that is inverted with respect to the tripping system ground. The voltage of this signal is proportional to the current in the transformer 509.

The A.C. rectified signal 558 is filtered by filter 560 for noise suppression and then inverted using analog invertor 562. From the analog invertor 562, a positive-going signal is carried to an A/D input at the microcomputer 120. The microcomputer 120 measures the peak levels at the output of the analog invertor 562 to detect the presence of a ground fault. A conventional voltage divider switch 564 is controlled by the microcomputer 120 to selectively reduce that signal by two thirds, as may be required under severe ground fault conditions. Preferred component values are, for example, 10 Kohms for resistors 565 and 567; 20 Kohms for resistor 569; 19.6 Kohms for resistor 573; 10 Kohms for resistor 575;

0.033 microfarads for capacitor 577; part No. LM124 for amplifier 579; and part No. BS170 for IGFET 581.

(3) Providing System Power

Power for the tripping system is provided directly from the current on lines 16, and current on any one of the lines 106 can be used. This feature allows the breaker unit to power-up on any one of the three phases and to be powered when a ground fault on one or more of the phase lines 16 is present. Furthermore, breaker unit 100 can be powered up or down from a remote location via the programmer 20.

The output currents which are induced by the transformers 510, 512 and 514 are routed through the rectifier bridges 516, 518, 520 and 522 to provide the current for the power supply 122. On the right side of the rectifier bridges 516-522, at lead 524, the output currents are summed and fed directly to a Darlington transistor 568, a 9.1 volt zener diode 570 and a bias resistor 572. Most of this current flows directly through the transistor 568 to ground, to create a constant 9.1 volt level at the base of the transistor 568. Because it has a nominal emitter to base voltage (Veb) of about 1.0 volts, the emitter of the transistor 568 is at approximately 10 volts. The transistor 568 will maintain 10 volts across it from emitter to collector, regardless of the current through it. Preferred component values are, for example, part No. 2N6285 for Darlington transistor 568; 1N4739 for zener diode 570; and 220 ohms for resistor 572.

The power signal VT ("trip voltage") is provided at the emitter of the transistor 568.

The +5v signal is a regulated +5v power supply output signal that is provided using a voltage regulator 571 (part No. LP2950ACZ-5.0) and a capacitor 582 which prevents the output of the regulator 571 from oscillating. The voltage regulator takes its input from VT via a diode 576. The diode 576 charges capacitor 584 to within one diode drop (0.6v) of VT and creates a second supply source of approximately +9v, which is referred to as the +9V power supply. The energy stored in the capacitor 584 enables the electronic circuitry being powered by the +9V power supply to remain powered for some time after a trip occurs. A capacitor 574, connected at the emitter of the transistor 568, aids in filtering voltage ripple. The capacitor 574 is also utilized as the energy storage element for the solenoid 112 which is activated when a power IGFET 583 is turned on by "trip" signals from the microcomputer (120 in FIG. 1b) or from a watchdog circuit (712 in FIG. 8). The trip signals are combined by respective diodes 591, 593. The solenoid 112 is also activated by an over-voltage condition sensed by a 16-volt zener diode 595, such as part No. 1N5246. Preferred component values are, for example, 220 microfarads for capacitor 574, 100 microfarads for capacitor 584, 10 microfarads for capacitor 582, 100 Kohms for resistor 585, 10 Kohms for resistor 589, 0.1 microfarads for capacitor 587, and part No. 6660 for IGFET 583.

Diodes 576 and 578 are used to receive current from an optional external power supply (not shown).

(4) Establishing The Current Rating

On the left side of the rectifier bridges, negative phase signals (A', B' and C') from the bridges are provided to the burden resistor arrangement 530,

including a rating plug 531, to set the current rating for the tripping system. As previously discussed, when the primary current is 100% of the rated current or "sensor size", which can be programmed via remote programmer 20 or user select circuit 132, the current transformer output current will be 282.8 milliamperes (RMS). Thus, when the microcomputer 120 reads the burden voltages using the gain circuit 134 (FIG. 1b), the microcomputer 120 can calculate the actual current in the lines 16.

FIG. 4 illustrates parallel connections between respective resistors 527 and 529 which are used to establish the maximum allowable continuous current passing through the lines 16. The resistors 527 are part of the rating plug 531, and the resistors 529 are separate from the rating plug 531. The resistors 529, for example, are each 4.99 ohm, 1%, 5 watt resistors. This value should be compared to a corresponding value of 12.4 ohms for the burden resistor 525 for the ground fault signal. The resistors 527 of the rating plug are connected in parallel with the resistors 529 and hence cause a decrease in the combined resistance. Therefore, the resistors 529 set the minimum current rating for the tripping system. In a preferred arrangement, for example, the minimum current rating corresponds to 40% of the maximum current rating. The resistors 527 in the rating plug scale the voltages (A', B', C') read by the microcomputer. This enables the resolution of the A/D converter in the microcomputer to be the same in terms of a fraction of the rated current for both the minimum and maximum current rating. Consequently, there is not any sacrifice in converter resolution for the minimum current rating.

In FIGS. 6a and 6b, the rating plug 531 is shown to include the resistors 527 mounted on a printed circuit board 587. A connector 588 is used to interconnect the rating plug with the remaining portion of the tripping system 100. When the rating plug is absent from the tripping system, the system reverts to its minimum rating.

The rating plug 531 further includes copper fusible printed circuit links A, B, C and D which are selectively disconnected (opened) from a printed circuit connection 589 to inform the microcomputer 120 of the resistor values, or the burden voltage/current ratio, in the burden resistor arrangement 530. The printed circuit connection 589 is connected to the +5V signal via one of the contact points on the connector 588. This connection 589 allows the tripping system to encode the printed circuit links A, B, C and D in binary logic such that one of 16 values of each parallel resistor arrangement is defined therefrom. In a preferred arrangement, the binary codes "1111" and "1110" are reserved for testing purposes, and the fourteen codes "0000" to "1101" correspond to current rating multipliers of 0.400 to 1.000 as follows:

Code	Current Rating Multiplier
0000	0.400
0001	0.500
0010	0.536
0011	0.583
0100	0.600
0101	0.625
0110	0.667

0111	0.700
1000	0.750
1001	0.800
1010	0.833
1011	0.875
1100	0.900
1101	1.000

The user select circuit 132 of FIG. 9 includes the interface circuit used by the microcomputer 120 to read the binary coded resistor value from the rating plug 531. A tri-state buffer 820 allows the microcomputer 120 to selectively read the logic level of each of the four leads representing the status of the four fusible printed circuit links on the rating plug 531. A logic high at the input of the buffer 820, provided by the connection between the fusible printed circuit link and +5V signal, indicates that the corresponding link is closed. A logic low at the input of the buffer 820, provided by pull-down resistors 826 at the input of the buffer 820, indicates that the corresponding link is open.

The fusible printed circuit links A, B, C and D may be opened using a current generator to send an excessive amount of current through the links, thereby causing the copper links to burn. This is preferably performed before the rating plug 531 is installed in the tripping system. Thus, once installed, the rating plug 531 automatically informs the microcomputer 120 of its resistor values, and there is no need to adjust any settings or otherwise inform the microcomputer of the type of rating plug being used. The microcomputer may adjust the values read from its A/D converter by a predetermined scale factor corresponding to the binary coded resistor value to compute actual current values which are independent of the resistor values in the rating plug 531.

C. <u>Bi-metal Deflection Simulation</u>

The microcomputer 120 is programmed to simulate accurately the bi-metal deflection mechanism that is commonly used in tripping systems that do not use microprocessors. This is accomplished by accumulating the squared values of the measured current samples that are sensed by the analog input circuit 108. The sum of the squared values of that current is proportional to the accumulated heat in the breaker unit 100.

To simulate the bi-metal deflection during cooling, the microcomputer 120 is programmed to decrement logarithmically the accumulated square of the current. In other words, during a sampling interval, the accumulated value A of $I(t)^2$ is decremented by an amount proportional to A to account for the fact that the rate of heat loss is proportional to the temperature of the power system conductors above ambient temperature. In particular, the temperature in the breaker unit 100 decreases if the current path in lines 16 is broken or intermittent. When this occurs, the microcomputer 120 loses operating power and can no longer maintain this numerical simulation.

This problem is overcome by utilizing the thermal memory 138 of FIG. 1b to maintain a history of the accumulated current for a predetermined period of time during which the operating power to the microcomputer 120 is lost. As illustrated in FIG. 7, this is accomplished using an RC circuit 610 that is monitored and controlled by the microcomputer 120 to maintain a voltage on the capacitor 611 that is proportional to the accumulated square of the current. When the microcomputer loses power, the voltage across the RC circuit 610 logarithmically decays. (The decay is governed by the equation $V = V_0 \exp(-t/RC)$.) Should the microcomputer power-up again before the voltage reaches

zero, the microcomputer 120 reads the voltage across the RC circuit 610 using a conventional analog buffer 612 and initializes its delay accumulator to the correct value. The analog buffer 612, for example, includes an amplifier 627 such as part No. LM714 and a 4.7 Kohm resistor 629.

The preferred RC circuit 610, including a 100 microfarad capacitor 611 and a 3.24 megohm resistor 613, provides a fixed time constant of 324 seconds, or approximately 5.4 minutes.

Control over the voltage on the RC circuit 610 is provided using IGFET transistors 618 and 620, such as part Nos. VP0808 and BS170, respectively. During normal, quiescent conditions, the microcomputer 120 will not be in an overload condition and will drive a logic low at the gate of the transistor 620, thereby disabling transistors 620 and 622 and allowing the capacitor 611 to discharge to tripping system ground. Transistors 618 and 620 work in connection with resistors 621, 623 and 625, which have values, for example, of 100 Kohms, 47 Kohms, and 5.1 Kohms, respectively.

During overload conditions, the microcomputer 120 accumulates current information in its internal RAM to simulate the heat level, and drives a logic high at the gate of the transistor 620 to allow the capacitor 611 to charge to a selected corresponding level. While the capacitor 611 is charging, the microcomputer 120 monitors the voltage level using the analog buffer 612. When the selected level is reached, the microcomputer drives a logic low at the gate of the transistor 620 to prevent further charging. The voltage on the capacitor 611 is limited to five volts using a clamping diode 622. The forward voltage drop across the clamping diode 622 is balanced by the voltage drop through a series diode 625.

For example, assume that an overload condition suddenly occurs and the microcomputer 120 has been programmed to allow for a two minute delay before generating a trip signal at this overload fault level. After one minute in this overload condition, the microcomputer 120 will have accumulated current information which indicates that it is 50% of the way to tripping. The microcomputer will also have enabled the RC circuit 610 to charge to 2.5v; that is, 50% of the maximum 5v. Assuming, for the purpose of this example, that the overload fault condition is removed at this point and the electronic trip system or breaker unit 100 loses operating power, when the power to the microcomputer 120 drops to Ov, the internally stored current accumulation is lost. However, the voltage across the RC circuit 610 is still present and will start to decay by approximately 63.2% every 5.4 minutes (the time constant for the RC circuit 610). Therefore, after 5.4 minutes without current, the voltage across the RC circuit 610 will be 36.8% of 2.5v, or 0.92v.

If the overload condition would occur again at this point, the microcomputer 120 would power up and measure 0.92v across the RC circuit 610. The microcomputer 120 would then initialize its internal current accumulation to approximately 18% (0.92v divided by the maximum of 5.0v) of the pre-programmed full trip delay time.

The accumulation calculations performed by the microcomputer are based on the formula:

$$A = \sum_{t=0}^{N} I(t)^2$$

where:

N = the number of samples;

t = time at discrete intervals (determined by the accumulation rate); and

I(t) = the true RMS value of current through the breaker.

During a fault, the trip unit will begin to sum the current squared value as soon as the current exceeds a predetermined level for a predetermined period of time, or the selected overload condition. The electronic trip system will maintain an internal accumulation register to store a value that is proportional to the square of the current and that is incremented periodically based on the accumulation rate. Assuming a constant fault level of current, a fixed accumulation rate, and a known condition of the accumulation register at t = 0, the value in the accumulation register will increase at a determinate rate and will contain a known value at any given time t.

For example, assume that a continuous fault is measured at 70.71 amperes (RMS) with an accumulation period of 64 milliseconds. Further assume that the accumulation register is at zero prior to the fault. The microcomputer 120 will accumulate the squared value of the current every 64 milliseconds into the register, causing it to increase at a constant rate.

With a continuous, fixed level fault, as time increases, the internal accumulation register increases proportionally. In order to protect the system from this fault, this increasing accumulated value is compared periodically against a predetermined threshold value that has been chosen to represent the maximum allowed heat content of the system. When the accumulated value equals or

exceeds this predetermined threshold value, the tripping system will trip the breaker.

A valuable aspect of accumulating the current squared value is that as the current doubles, the current squared value quadruples and the internal accumulation register increases at a more rapid rate, resulting in a more rapid trip. Thus, if the delay time (the period before the detected power fault causes a trip) is x seconds at some current level, as the current doubles, the delay time will be x/4 seconds.

The formula for calculating the delay time for any constant current is:

$$T = \frac{A_R \times K}{I^2}$$

where:

A_R = the accumulation rate in seconds;

K = predetermined final accumulation value; and

I = the true RMS value of current flowing through the breaker.

D. Reset Circuitry

Referring now to FIG. 8, an expanded view of the reset circuit 124 is shown to include a power-up reset circuit 710 and a watch-dog circuit 712 to maintain the integrity of the tripping system 100. The power-up reset circuit 710 performs two functions, both of which occur during power-up: it provides a reset signal (asserted low) on line 743 to maintain the microcomputer 120 in reset condition until the tripping system 100 develops sufficient operating power from the current lines 106; and it provides a reset signal (asserted low) via lead 744 to

the watch-dog circuit 712 to prevent the watch-dog circuit from engaging the solenoid 112 during power-up. This function prevents nuisance tripping.

Preferably the power-up reset circuit includes an under-voltage sensing integrated circuit 745 that detects whether or not the output voltage of the +5 volt supply is less than a predetermined reference voltage at which the microcomputer (120 in FIG. 1b) may properly function. The integrated circuit 745 is, for example, part No. MC33064P-5, which holds the reset line 743 low until the output voltage of the +5 volt supply rises above 4.6 volts. The microcomputer 120 may operate at 4.5 volts or above. The preferred reset circuit also includes a pull-up resistor 741, a capacitor 739, and a diode 753 connecting the integrated circuit 745 to the watchdog circuit 712. The resistor 741, for example, has a value of 47 Kohms and the capacitor 739 has a value of 0.01 microfarads. The diode 753 ensures that the reset circuit 710 affects the watchdog circuit 712 only when the microcomputer 160 is being reset.

The watch-dog circuit 712 protects the tripping system from microcomputer malfunctions. Thus, it is designed to engage the solenoid 112 if the microcomputer 120 fails to reset the watch-dog circuit 712 within a predetermined time period. The microcomputer 120 resets the watch-dog circuit 712 by regularly generating logic high pulses, preferably about every 200 milliseconds, on lead 714. These pulses are passed through a capacitor 718 to activate an IGFET transistor 720, which in turn discharges an RC timing circuit 724 through a circuit limiting resistor 733. A resistor 730 and a clamping diode 732 are used to reference the pulses from the capacitor 718 to ground.

The pulses on lead 714 prevent the RC timing circuit 724 from charging up past a reference voltage, Vref, at the input of a comparator 726. If the RC timing circuit 724 charges past Vref, the comparator 726 sends a trip signal to the solenoid 112 to interrupt the current path in lines 106. The reference voltage, for example, is provided by a 4.3 volt zener diode 427 supplied with current through a resistor 729. Preferred component values are, for example, 0.001 microfarads for capacitor 718, 27 Kohms for resistor 730, part No. 1N4148 for diode 732, part No. BS170 for transistor 720, 10 ohms for resistor 733, 0.22 microfarads for capacitor 735, part No. LM29031 for comparator 726, part No. 1N4687 for diode 727, 100 Kohms for resistor 729, and 10 Kohms for resistor 751.

E. User Select Switches

As introduced above, the user select circuit 132 is illustrated in FIG. 9. In addition to the buffer 820 for the rating plug, the user select circuit 132 includes a plurality of user interface circuits 810 each having a pair of BCD dials 812 and a tri-state buffer 814 which is enabled through the address and data decoder 130 of FIG. 1b. Each BCD dial 812 allows the user to select one of several tripping system characteristics. For example, a pair of BCD switches may be used to designate the longtime pickup and the longtime delay (overload tripping characteristics) and another pair of BCD switches may be used to designate the short time pickup and the short time delay (short circuit tripping characteristics). Other BCD switches may be used to designate sensor and breaker sizes, an instantaneous pickup, ground fault tripping characteristics, and phase unbalance thresholds.

F. Energy Validation For Solenoid Activation

The user select circuit 132 of FIGS. 1b and 9 also determines if there is sufficient energy to activate the solenoid 112. Using the address and data decoding circuit 130, the buffer 820 is selected to read one of its input lines 830. The VT signal from the power supply 122 of FIG. 1b feeds the input line 830, with the buffer 820 being protected from excessive voltage by a resistor 832 and a clamping diode 834. The resistor 832, for example, has a value of 620 Kohms.

Before the microcomputer 120 engages the solenoid 112, the input line 830 is accessed to determine if VT is read as a logic high or a logic low. The buffer 820 provides a logic high at its output whenever the input is greater than 2.5v to 3v. If VT is read as a logic high, the microcomputer 120 determines that there is sufficient power to activate the solenoid 112 and attempts to do so. If VT is read as a logic low, the microcomputer 120 determines that there is insufficient power to activate the solenoid 112 and waits, while repeatedly checking VT, in anticipation that an intermittent power fault caused VT to fall. Once VT rises beyond the 2.5-3.0 volt level, the microcomputer 120 attempts to activate the solenoid once again.

G. Communication For Information Display

The microcomputer 120 sends identical tripping system status information to the local display 150 and the display terminal 162. The information is sent synchronously on a serial peripheral interface 191 to the local display 150 and asynchronously on a serial communication interface 151 to the display terminal 162. The interfaces 151 and 191 may be implemented using the SCI and SPI ports internal to the MC68HC11.

The history of the tripping system status information is stored in the nonvolatile trip memory 144. That history includes the specific cause and current level of the last trip and a running accumulation of the different trip causes.

The trip memory 144 is preferably an electrically erasable programmable ROM (EEPROM), for example, a X24CO4I, available from Xicor, Inc. of Milpitas, California. In this case, the serial peripheral interface 191 is used for bidirectional data transfer between the microcomputer 120 and the EEPROM 144. This data transfer is implemented using one line of the serial peripheral interface 191 to transfer the data and the other line to transmit a clock signal between the microcomputer 120 and the EEPROM 114 for synchronization. During power up of the tripping system 100, the microcomputer 120 transmits to the trip memory 144 a unique bit pattern which is interpreted as a data request code. The microcomputer 120 then sets the bidirectional data line as an input and clocks the requested data in from the trip memory 144.

The microcomputer 120 maintains a copy of the history data in its internal RAM and in the event of a trip, updates it and transmits it back into trip memory 144 via the interface 191, again utilizing the unique bit pattern to set the trip memory 144 to a receive mode. Upon receipt of the data, trip memory 144 will reprogram its contents, overwriting the old history information with the newly received data.

During normal operation (i.e., after power up and without a trip), the microcomputer 120 transmits operational information over the serial peripheral interface 191. Because this information does not contain the unique bit patterns required to activate the trip memory 144, the trip memory 144 ignores the normal

transmissions. However, other devices which may be connected to the serial peripheral interface 191 can receive and interpret the information correctly.

The microcomputer 120, for example, is programmed to execute a communication procedure that permits the tripping system 100 to communicate with a relatively low power processor in the display processor 316. The procedure utilizes a software interrupt mechanism to track the frequency with which information is sent on the interfaces 151 and 191. During normal operation, one 8-bit byte of information is sent every seven milliseconds. During tripping conditions, information is sent continuously as fast as the microcomputer 120 can transmit. This procedure allows the display terminal 162 and the display processor 316 to continuously display status messages from the tripping system 100 without dedicating their processors exclusively to this reception function. Equally important, this procedure permits the microcomputer 120 to perform a variety of tasks, including continuous analysis of the current on lines 106.

Status messages are preferably transmitted using an 8-byte per packet, multi-packet transmission technique. The type of information included in each packet may be categorized into eight different groups, or eight different packets, packet 0 through packet 7. The first byte of each packet is used to identify the byte and packet numbers and the trip status of the tripping system 100. For example, the first byte may contain one bit to identify the byte type, four bits to identify the packet number and three bits to identify the trip status: no trip condition, current overload trip, short circuit trip, instantaneous trip, ground fault trip and phase unbalance trip. Bytes two through six of each packet vary depending on the packet number. Byte 7 is used to identify the tripping system

sending the information (for a multiple system configuration), and byte 8 is used as a checksum to verify the integrity of the data.

The microcomputer alternates the type of information included in each packet, depending upon the priority type of the information. During normal (non-tripping) conditions, the trip unit will transmit Packet Number 0, followed by Packet Number 1, followed by one of the remaining defined Packet Numbers, 2 through 7. The sequence is graphically shown as:

1)	Packet 0 - Packet 1 - Packet 2	
2)	Packet 0 - Packet 1 - Packet 3	
3)	Packet 0 - Packet 1 - Packet 4	Repeat until Trip
4)	Packet 0 - Packet 1 - Packet 5	Occurs
5)	Packet 0 - Packet 1 - Packet 6	
6)	Packet 0 - Packet 1 - Packet 7	

During a trip condition, the normal operation packet transmission sequence is interrupted and Packet number 2 is transmitted continuously until power is lost. The transmission rate will be increased to the fastest rate possible.

The five bytes of each packet that vary according to packet number are configured for a total of eight different packets, 0-7. The information in these bytes is implemented for each packet number as follows:

Packet 0 - (0 0 0 0)
Data Byte 1 - Phase A Current - High Byte
Data Byte 2 - Phase A Current - Low Byte
Data Byte 3 - Phase B Current - High Byte
Data Byte 4 - Phase B Current - Low Byte
Data Byte 5 - Overload Pickups & Short Circuit Restraint In

Packet 1 - (0 0 0 1)
Data Byte 1 - Phase C Current - High Byte

Data Byte 2 - Phase C Current - Low Byte
Data Byte 3 - Ground Fault Current - High Byte
Data Byte 4 - Ground Fault Current - Low Byte
Data Byte 5 - Short Circuit, Phase Unbalance & Ground Fault Pickups

Packet 2 - (0 0 1 0)
Data Byte 1 - Maximum Phase Current - High Byte
Data Byte 2 - Maximum Phase Current - Low Byte
Data Byte 3 - Maximum Phase Identification (A, B, C or N), Breaker Identification & Ground Fault Restraint In
Data Byte 4 - Trip Unit/Sensor Identification
Data Byte 5 - Rating Plug/Options

Packet 3 - (0 0 1 1)
Data Byte 1 - Long Time Switches
Data Byte 2 - Short Time Switches
Data Byte 3 - Instantaneous Phase Unbalance Switches
Data Byte 4 - Ground Fault Switches
Data Byte 5 - Phase Unbalance Trips

Packet 4 - (0 1 0 0)
Data Byte 1 - Long Time Trips
Data Byte 2 - Short Circuit Trips
Data Byte 3 - Ground Fault Trips
Data Byte 4 - Last Maximum Phase Current - High Byte
Data Byte 5 - Last Maximum Phase Current - Low Byte

Packet 5 - (0 1 0 1)
Data Byte 1 - Software Failure Trips
Data Byte 2 - Last Phase A Current - High Byte
Data Byte 3 - Last Phase A Current - Low Byte
Data Byte 4 - Last Phase B Current - High Byte
Data Byte 5 - Last Phase B Current - Low Byte

Packet 6 - (0 1 1 0)
Data Byte 1 - Last Fault System Status Byte
Data Byte 2 - Last Phase C Current - High Byte
Data Byte 3 - Last Phase C Current - Low Byte
Data Byte 4 - Last Ground Fault Current - High Byte
Data Byte 5 - Last Ground Fault Current - Low Byte

Packet 7 - (0 1 1 1)
Data Byte 1 - Long Time Memory Ratio
Data Byte 2 - Phase A % Unbalance

Data Byte 3 - Phase B % Unbalance
Data Byte 4 - Phase C % Unbalance
Data Byte 5 - Software Version Identifier Byte

Accordingly, the microcomputer 120 transmits information in four substantive classes. The first class constitutes trip status information, as set forth in the first byte of each packet. The second and third classes involve current measurement information; the second class including current measurement information on each line 106, as set forth in packets 0 and 1, and the third class including the maximum current status information, as set forth in packet 2. The last class of information relates to the present configuration of the tripping system and is contained in packets 3 through 7.

Referring to Figure 10b, a flow diagram is shown illustrated the preferred algorithm for the configuration programming protocol described above. The diagram begins at block 860 where the user programs via remote programmer 20, a request to send a program sequence with new set of trip points or configuration signals into tripping system 10. The user then may transmit the requested program to system 10 via communication channel 870. Thus, Figure 10b illustrates a dotted line indicating activities to the left of the dotted line within remote programmer 20 and activities to the right of the dotted line within tripping system 10. Transmission of new trip points, etc. comprises optical configuration signals 22, as shown in Figure 1a, to system 10, wherein system 10 temporarily buffers the transmitted data at block 861 and checks the data or configuration signals for valid transmission as shown in block 862. If the data checks good, then the data is transmitted back to the remote programmer 863 indicating that the request was successfully received. If the data does not check good, error

information is transmitted to the remote programmer and the programmer must resend the program sequence as shown in block 864. Blocks 863, 864 and 865 look for successful transmission of program requests. Upon determining if tripping system 10 received a valid request to change configuration trip points at block 864, the remote programmer 20 transmits a store command to the tripping system 10 to instruct the tripping system to save the new data into its non-volatile configuration memory. The tripping system then stores the data at block 866 and in block 867 returns to executing normal circuit breaker protection code in transmitting the normal serial communication.

The flow diagram of the Figure 10b illustrates an example of the self-checking mechanism by which remote programmer 20 can insure that selective breaker units 100 operate correctly. If a breaker unit 100 fails to operate upon receiving remote programming commands, that unit 100 can be identified back to the remote programmer 20 thereby informing the field user. As shown in block 865, specific defective breaker units 100 can be identified and information transmitted back to the operator. If, however, the identified units correctly receive programmed code such as, *e.g.*, remotely programmed trip points, then the selected unit 100 will receive configuration data within the microcomputer's non-volatile memory, preferably EEPROM as shown in block 866. To verify accurate receipt of transmitted data, the selected unit 100 sends back to the remote programmer the received data stream after 250 milliseconds as shown in block 867. The programmer then waits for all packets of data to verify correct storage of the configuration data, including trip points, ZSI data, etc. as shown in block 868. Once all packets are verified, remote programmer 20 then informs the

operator that correct breaker, sensor and ZSI data is received and that the programming protocol is operating correctly as shown in block 869.

WHAT IS CLAIMED IS:

1. A remotely programmable breaker unit, comprising:

a three-phase current path;

a trip solenoid means for breaking said current path;

a microcomputer coupled between said current path and said trip solenoid, said microcomputer including nonvolatile, remotely-programmable memory means for storing trip points which are used by the microcomputer to activate said trip solenoid when current within said current path exceeds at least one of said trip points; and

a remote programmer means, optically coupled to said microcomputer, for remotely programming said trip points, for storage in said nonvolatile, remotely-programmable memory means, said remote programmer means including a serial communication interface connected to said microcomputer via a remote program interface, and includiding keying means for transmitting an optical configuration signal to said microcomputer and for changing said stored trip points according to said optical configuration signal.

2. The breaker unit as recited in claim 1, wherein said remote programmer means comprises a display for receiving from said microcomputer a configuration signal corresponding to said trip points.

3. The breaker unit as recited in claim 1, wherein said microcomputer includes means for storing said trip points in a redundant form in said nonvolatile, remotely-programmable memory means such that upon an inadvertant loss of trip point data therein said microcomputer recovers an error-free copy of said data from said nonvolatile, remotely-programmable memory means.

4. The breaker unit as recited in claim 4, wherein said display comprises means for displaying current readings transmitted from said current path.

5. The breaker unit as recited in claim 1, further comprising:

a trip system housing for containing said trip solenoid means and said microcomputer;

a local display for locally presenting said trip points at a first location upon said trip system housing; and

a user select circuit for locally changing said trip points at a second location upon said trip system housing.

6. The breaker unit as recited in claim 1, wherein said trip points comprise a ground fault current magnitude equal to zero amperes within all of said three phase current path.

7. A programmable electronic trip system comprising:

a three phase current path;

a downstream trip unit including:

three current sensors, each sensor coupled to said three phase current path for sensing a respective phase of current there jnn;

a microcomputer coupled to said sensor, said microcomputer including:

summation means for adding an AC current transmitted through all said three current sensors,

detector means for measuring an RMS current,

a remote programmer means coupled to said microcomputer for selectively activating said summation means and said detector means in response to a ground fault condition and a short circuit condition, respectively, on said current path; and

a downstream trip solenoid means for breaking said current path when the output of said summation means and said detector means exceeds a plurality of stored trip points.

8. The trip system as recited in claim 7, further comprising:

an upstream trip unit connected to said downstream trip unit via a single electrical conductor;

a restraint out circuit connected to said microcomputer for generating a ground fault restraint out signal over said single electrical conductor to said upstream trip unit when the output of said summation means exceeds said stored trip points; and

said upstream trip unit having an upstream trip solenoid means for breaking said current path after expiration of a delay period upon receipt of said ground fault restraint out signal.

9. The trip system as recited in claim 7, further comprising:

an upstream trip unit connected to said downstream trip unit via a single electrical conductor;

a restraint out circuit connected to said microcomputer for generating a short circuit restraint out signal over said single electrical conductor to said upstream trip unit when the output of said detector means exceeds said stored trip points; and

said upstream trip unit having an upstream trip solenoid means for breaking said current path after expiration of a delay period upon receipt of said short circuit restraint out signal.

10. The trip system as recited in claim 7, wherein said trip points comprise a ground fault current magnitude stored in a random access memory within said microcomputer.

11. The trip system as recited in claim 7, wherein said trip points comprise a short circuit current magnitude stored in a random access memory within said microcomputer.

12. The trip system as recited in claim 7, wherein said remote programmer means comprises a keyboard for transmitting an optical configuration signal to said microcomputer to change said stored trip points according to said optical configuration signal.

13. The trip system as recited in claim 7, wherein said remote programmer means comprises a display for receiving from said microcomputer an optical configuration signal corresponding to said stored trip points.

14. A method for remotely programming ground fault trip characteristics and short circuit trip characteristics in a trip system, comprising:

providing a three phase current path having a current source and current load coupled at opposite ends of said current path;

coupling at least two programmable breakers to said current path between said source and load;

interconnecting said breakers with a single interconnect line;

remotely programming at least one said breaker to break said current path when said current path receives current fluctuations which exceeds a set of trip points stored within said respective breaker; and

transmitting a restraint out signal from one said breaker to the other said breaker over said single interconnect line.

15. The method as recited in claim 14, wherein one said breaker is a downstream breaker connected nearer said load than said other said breaker.

16. The method as recited in claim 14, wherein said step of remotely programming comprises:

optically coupling a remote programmer to one said breaker; and

inputting said set of trip points into said respective breaker from said remote programmer.

17. The method as recited in claim 14, wherein said step of remotely programming comprises:

optically coupling a remote programmer to one said breaker; and

displaying said set of trip points from said respective breaker to said remote programmer.

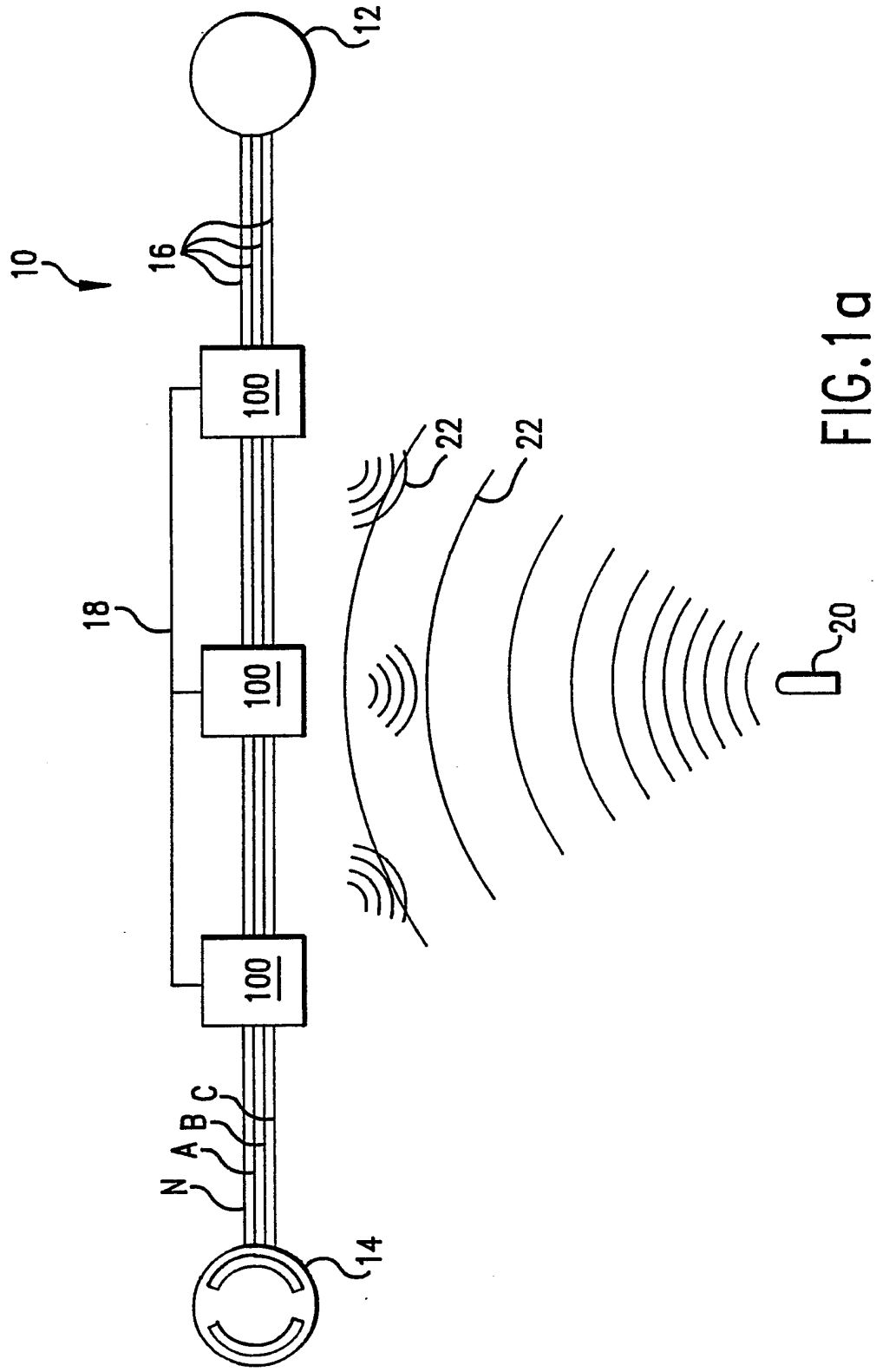


FIG. 1a

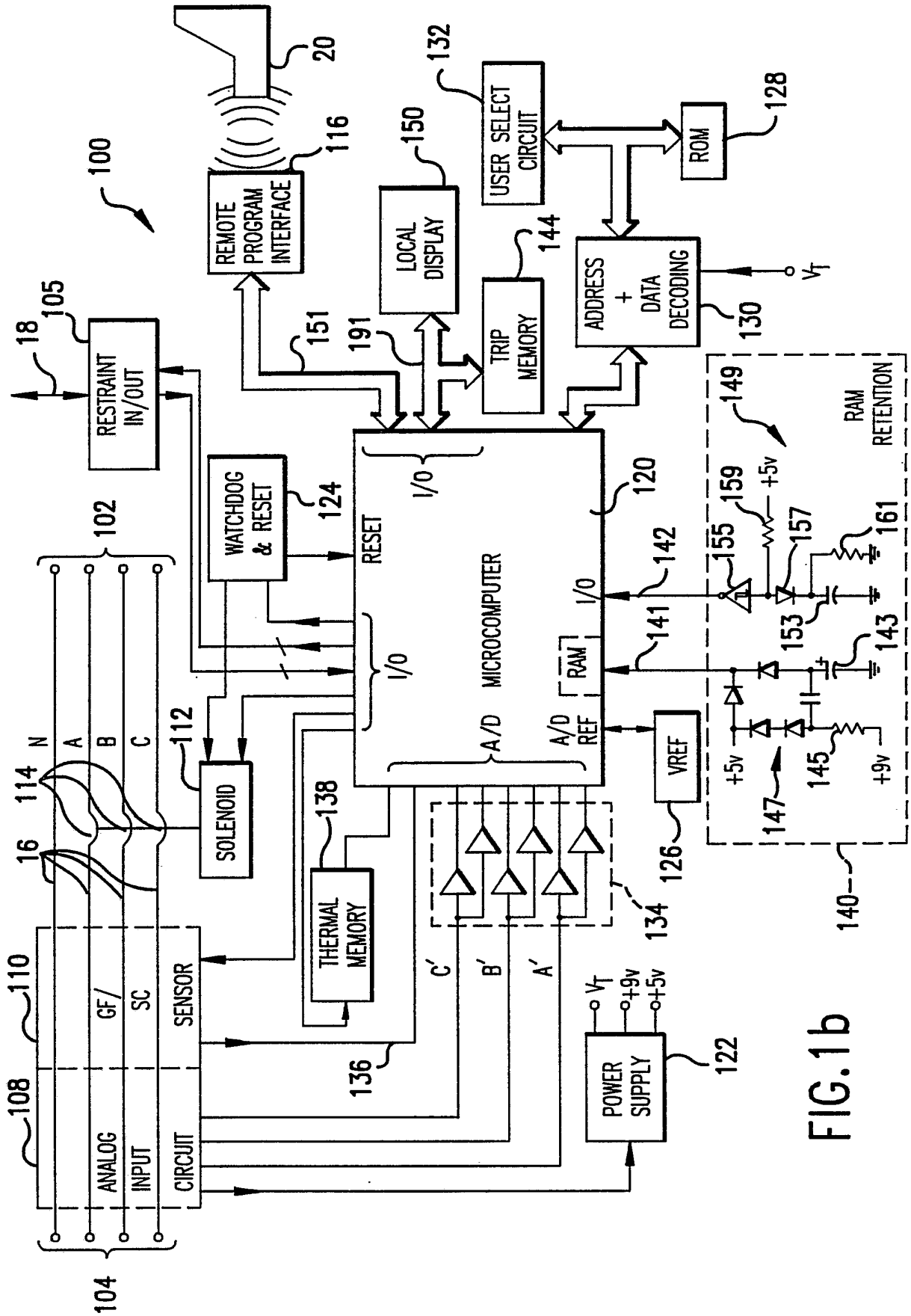

100
20
116
REMOTE PROGRAM INTERFACE
150
LOCAL DISPLAY
132
USER SELECT CIRCUIT
128
ROM
144
TRIP MEMORY
ADDRESS + DATA DECODING
130
V_T
105
18
RESTRAINT IN/OUT
151
191
WATCHDOG & RESET
124
RESET
I/O
120
MICROCOMPUTER
RAM
I/O
A/D
A/D REF
149
RAM RETENTION
159
+5v
155
157
161
142
141
153
143
102
112
SOLENOID
138
THERMAL MEMORY
VREF
126
134
140
147
145
+9v
+5v
N
A
B
C
114
16
110
108
SENSOR
GF/
SC
ANALOG
INPUT
CIRCUIT
104
C'
B'
A'
136
V_T
+9v
+5v
POWER SUPPLY
122

FIG. 1b

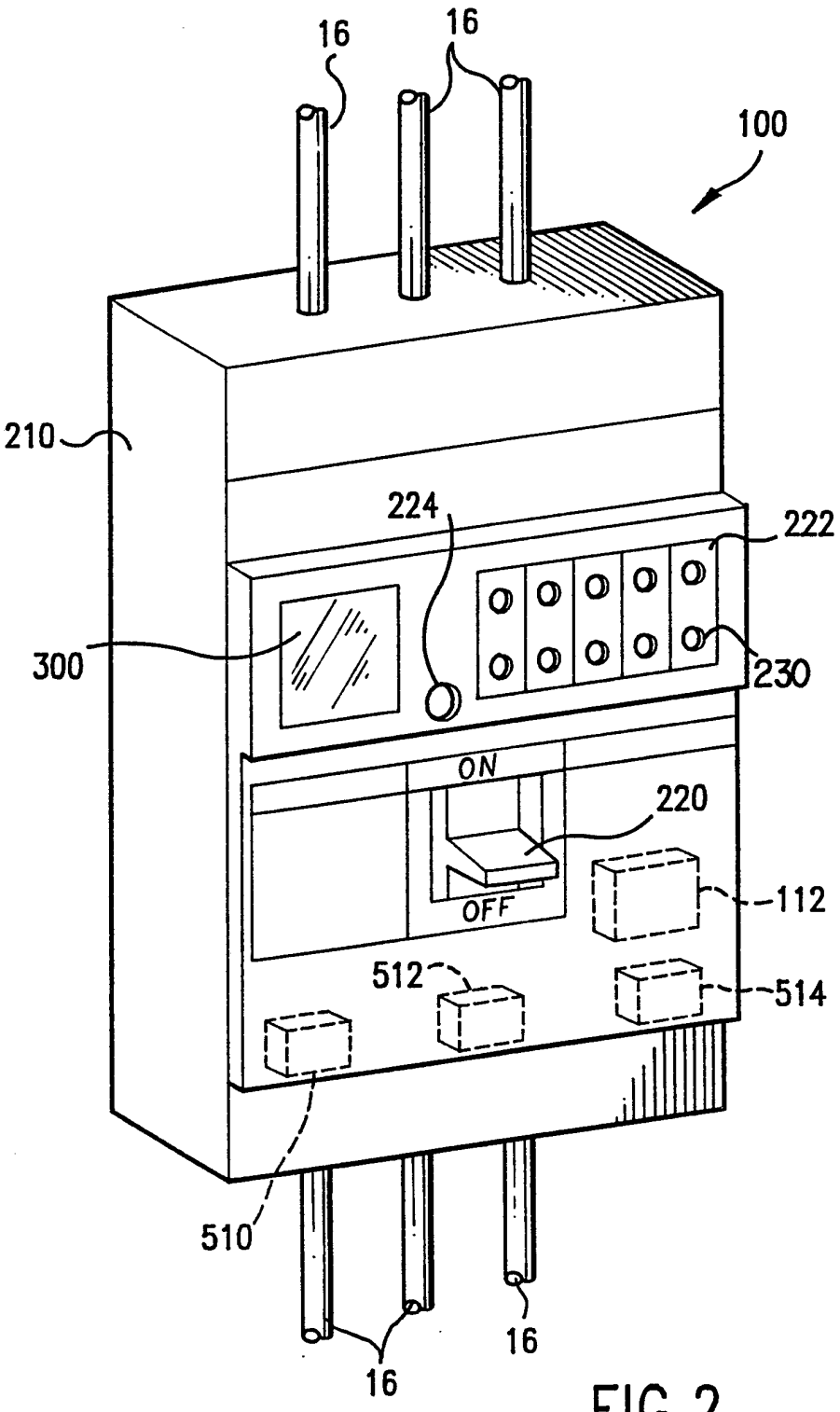


FIG.2

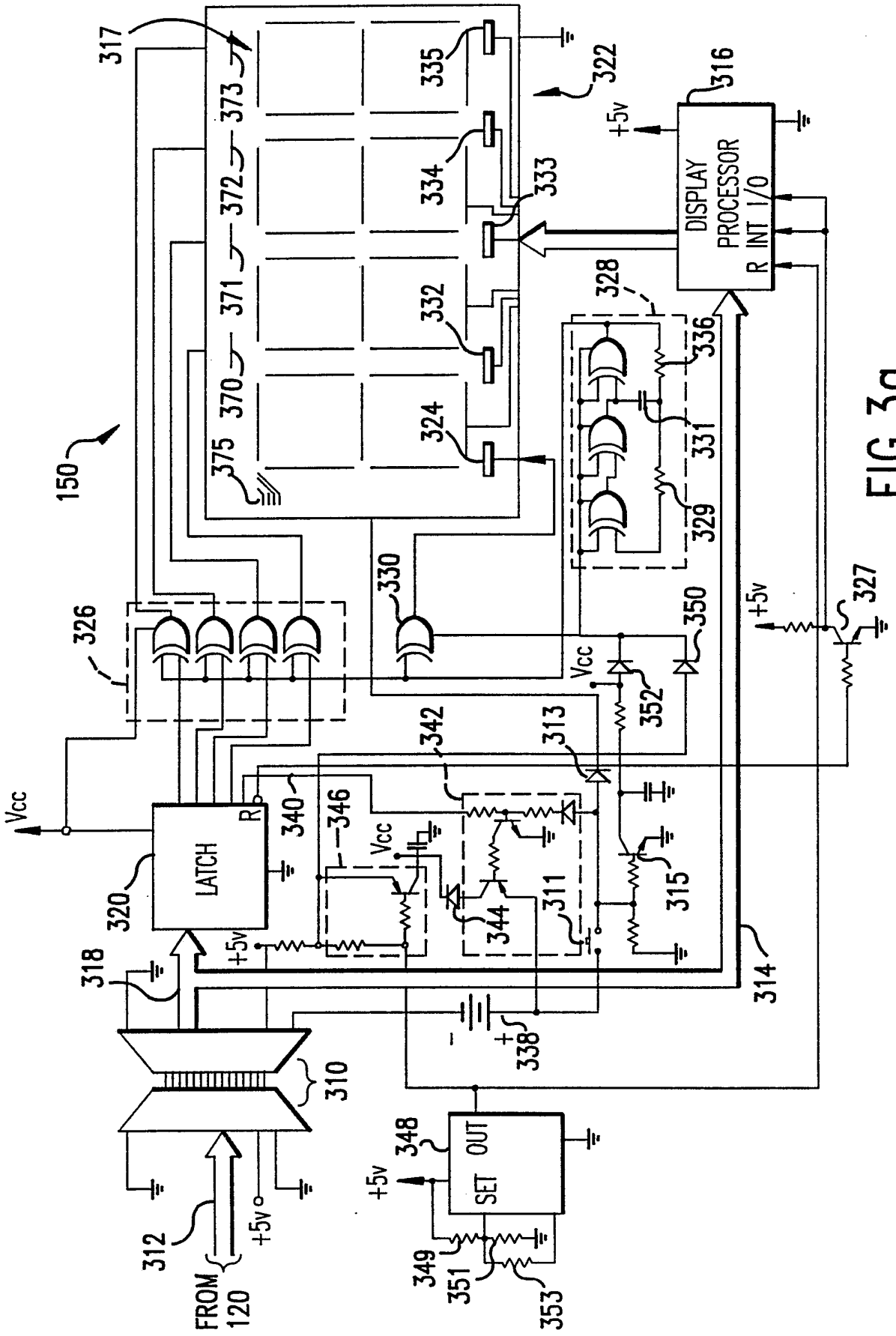

317
373
372
371
370
375
335
334
332
324
322
316
+5v
DISPLAY PROCESSOR R INT I/O
333
328
336
331
329
150
330
326
350
+5v
327
Vcc
352
342
313
340
346
Vcc
LATCH
R
320
+5v
318
344
311
315
314
338
310
348
+5v
SET OUT
312
FROM 120
+5v
349
351
353

FIG.3a

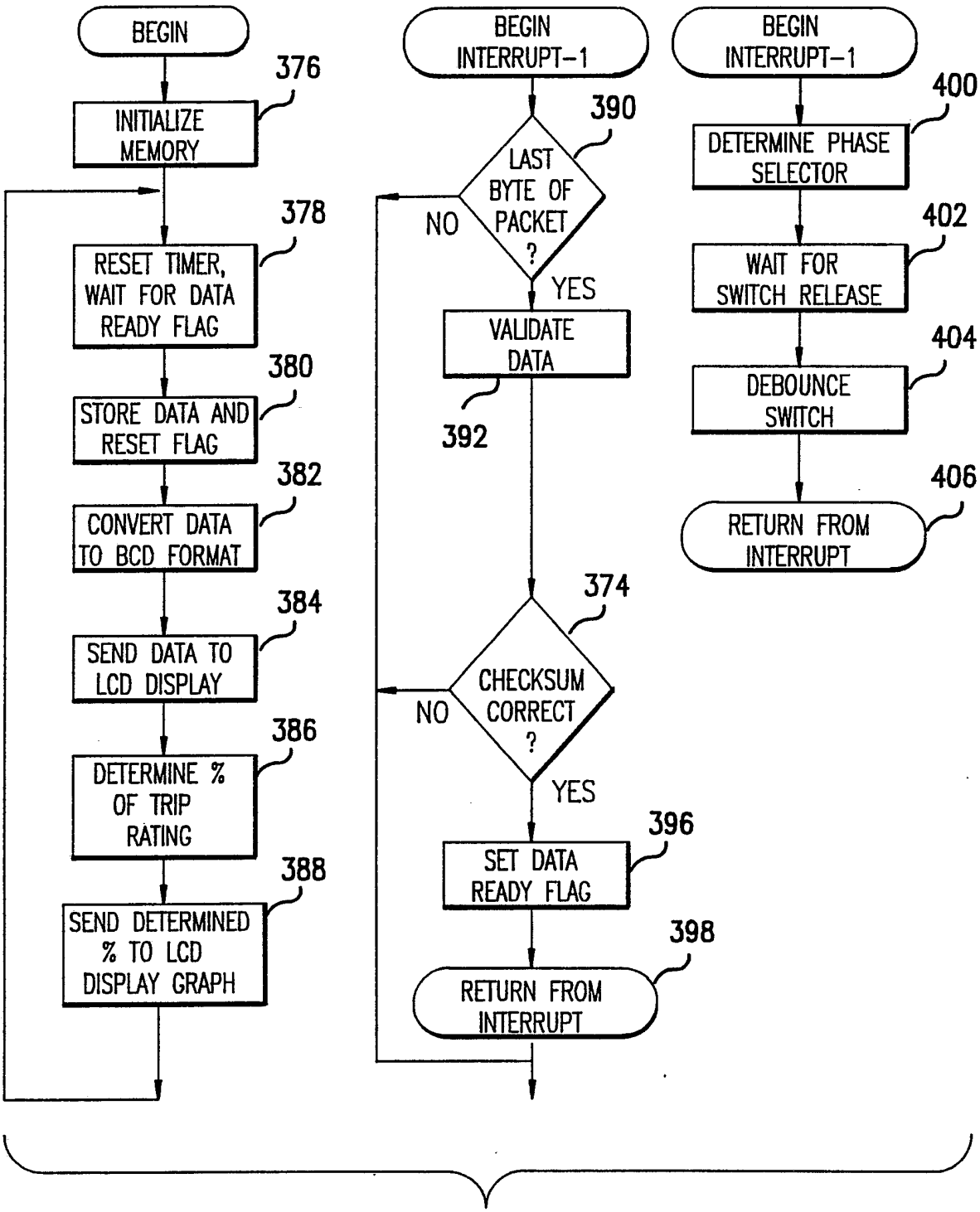

BEGIN
376
INITIALIZE MEMORY
378
RESET TIMER, WAIT FOR DATA READY FLAG
380
STORE DATA AND RESET FLAG
382
CONVERT DATA TO BCD FORMAT
384
SEND DATA TO LCD DISPLAY
386
DETERMINE % OF TRIP RATING
388
SEND DETERMINED % TO LCD DISPLAY GRAPH
BEGIN INTERRUPT-1
390
LAST BYTE OF PACKET ?
NO
YES
VALIDATE DATA
392
374
CHECKSUM CORRECT ?
NO
YES
396
SET DATA READY FLAG
398
RETURN FROM INTERRUPT
BEGIN INTERRUPT-1
400
DETERMINE PHASE SELECTOR
402
WAIT FOR SWITCH RELEASE
404
DEBOUNCE SWITCH
406
RETURN FROM INTERRUPT

FIG.3b

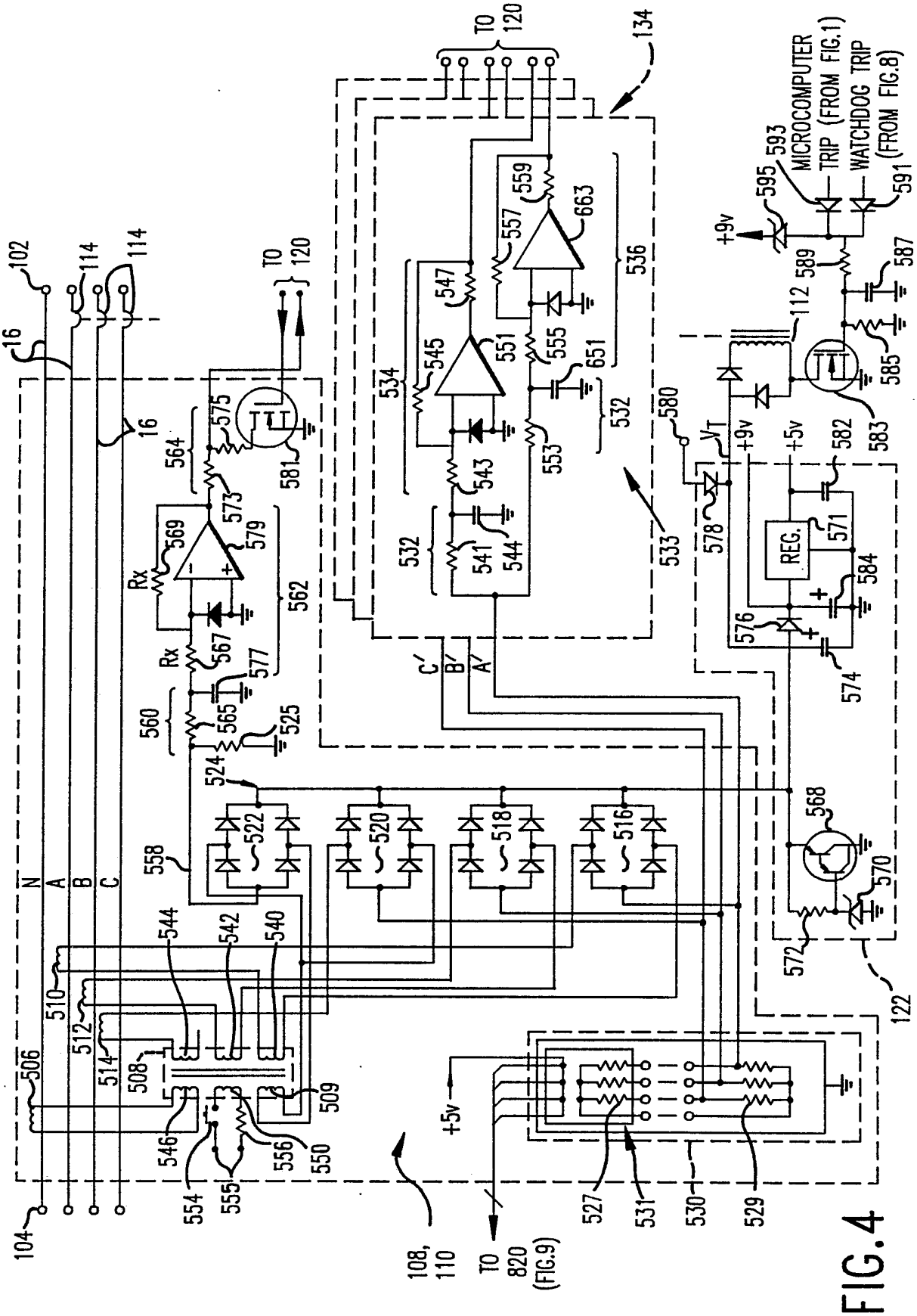

TO 120
134
MICROCOMPUTER TRIP (FROM FIG.1)
WATCHDOG TRIP (FROM FIG.8)
+9v
+5v
REG.
N
A
B
C
TO 820 (FIG.9)
108, 110
104
122

FIG. 4

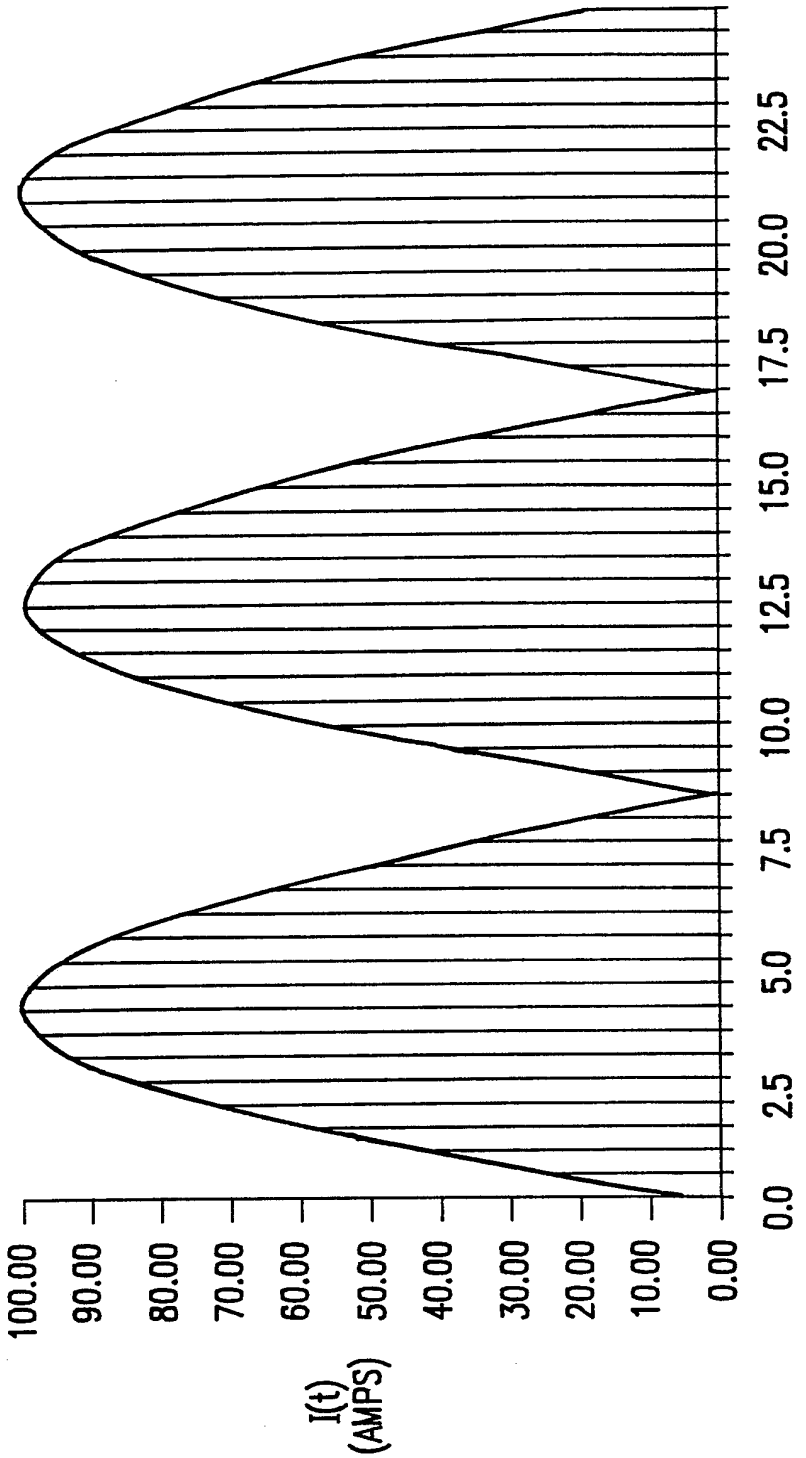

100.00
90.00
80.00
70.00
60.00
50.00
40.00
30.00
20.00
10.00
0.00
I(t)
(AMPS)
0.0
2.5
5.0
7.5
10.0
12.5
15.0
17.5
20.0
22.5
TIME (ms)

FIG.5

FIG.6a

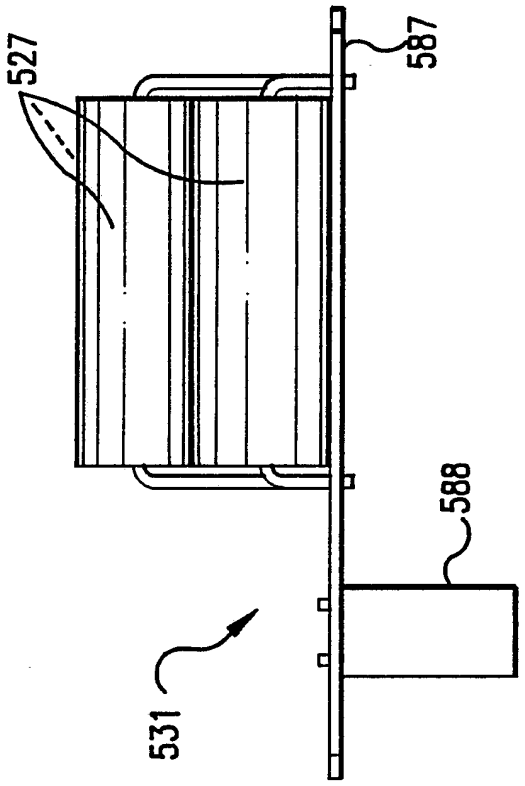
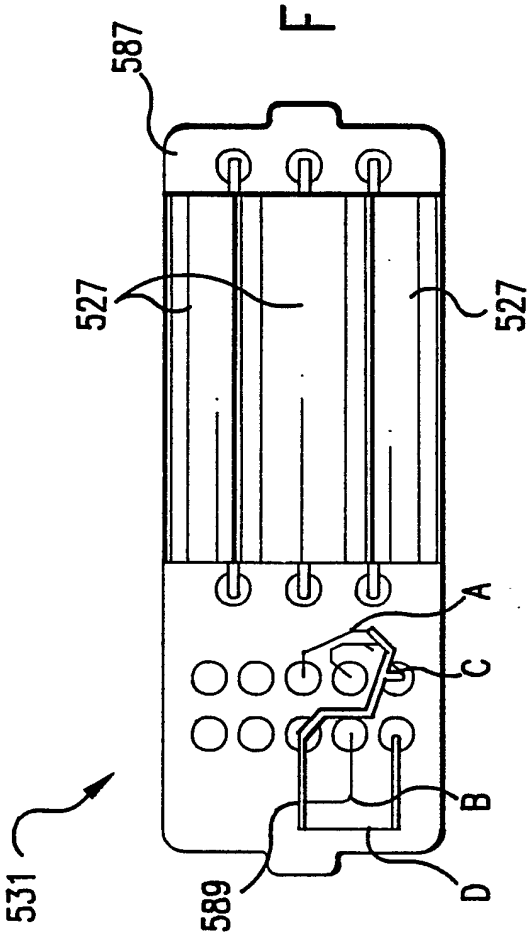


FIG.6b



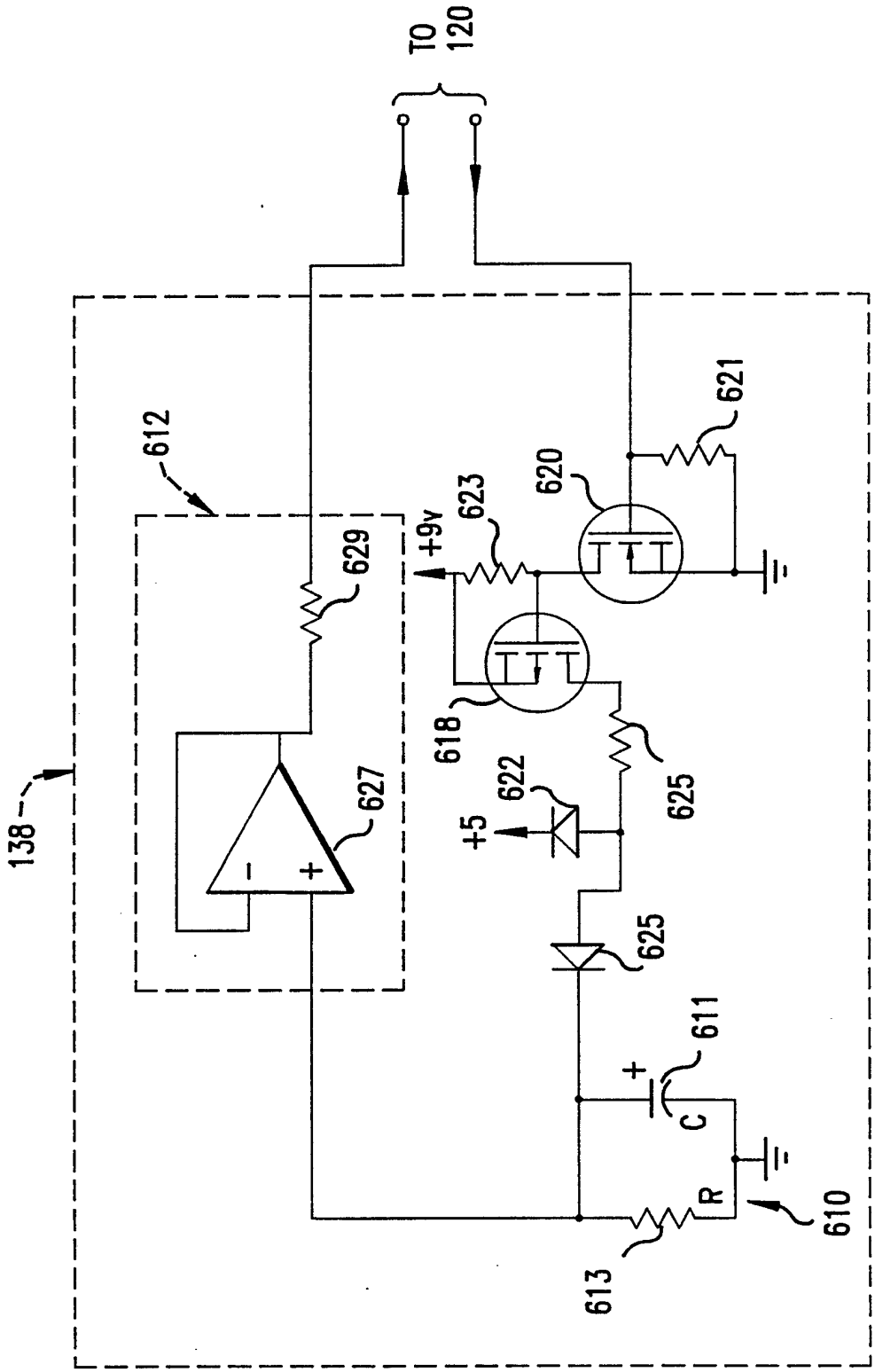

TO 120
612
621
620
623
+9v
629
618
625
622
+5
627
138
625
611
C
R
610
613

FIG. 7

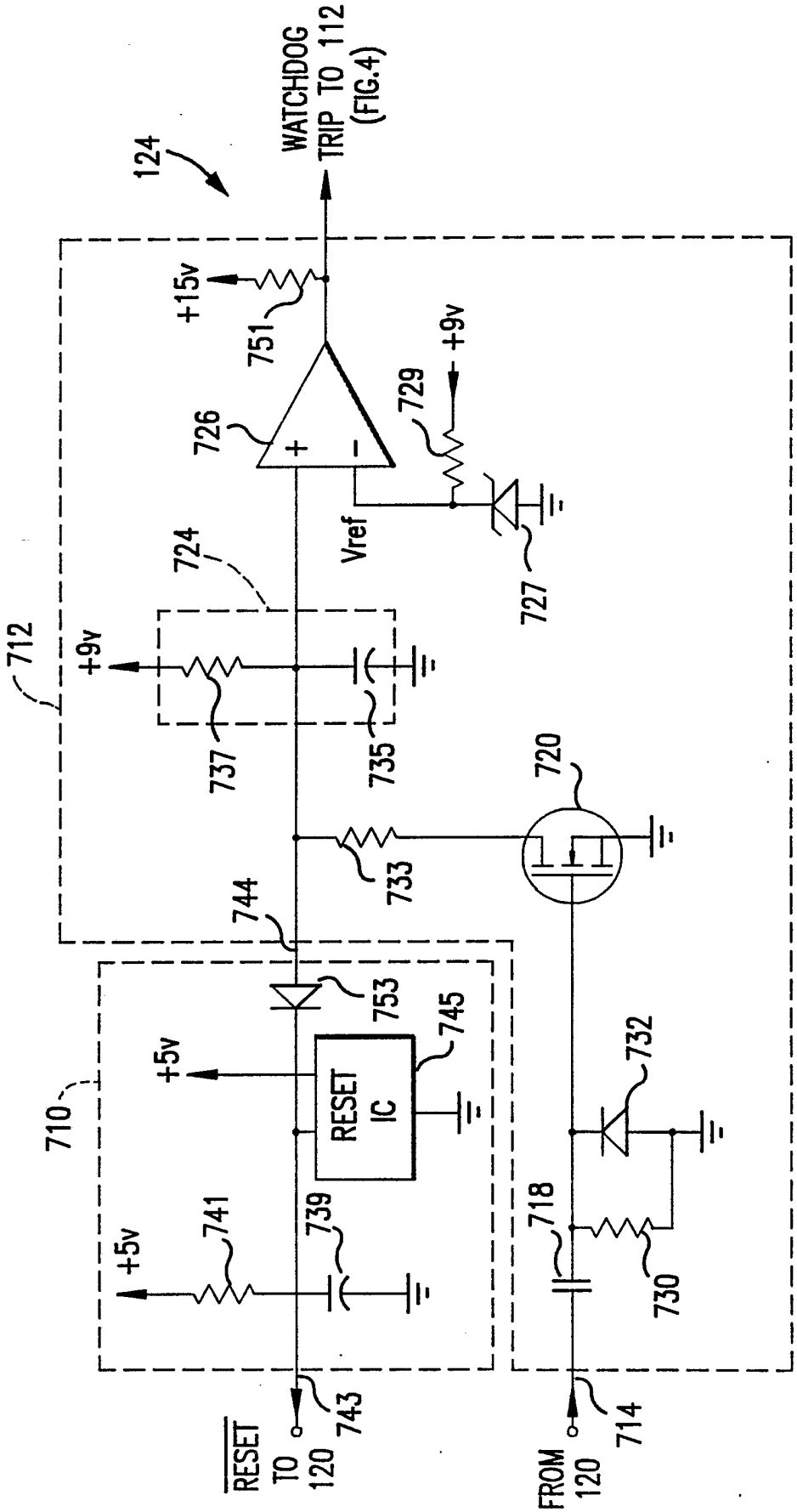

WATCHDOG TRIP TO 112 (FIG.4)
124
+15v
751
+9v
729
726
Vref
727
724
712
+9v
737
735
720
733
744
753
745
+5v
RESET IC
710
732
+5v
741
739
718
730
RESET TO 120
743
FROM 120
714

FIG.8

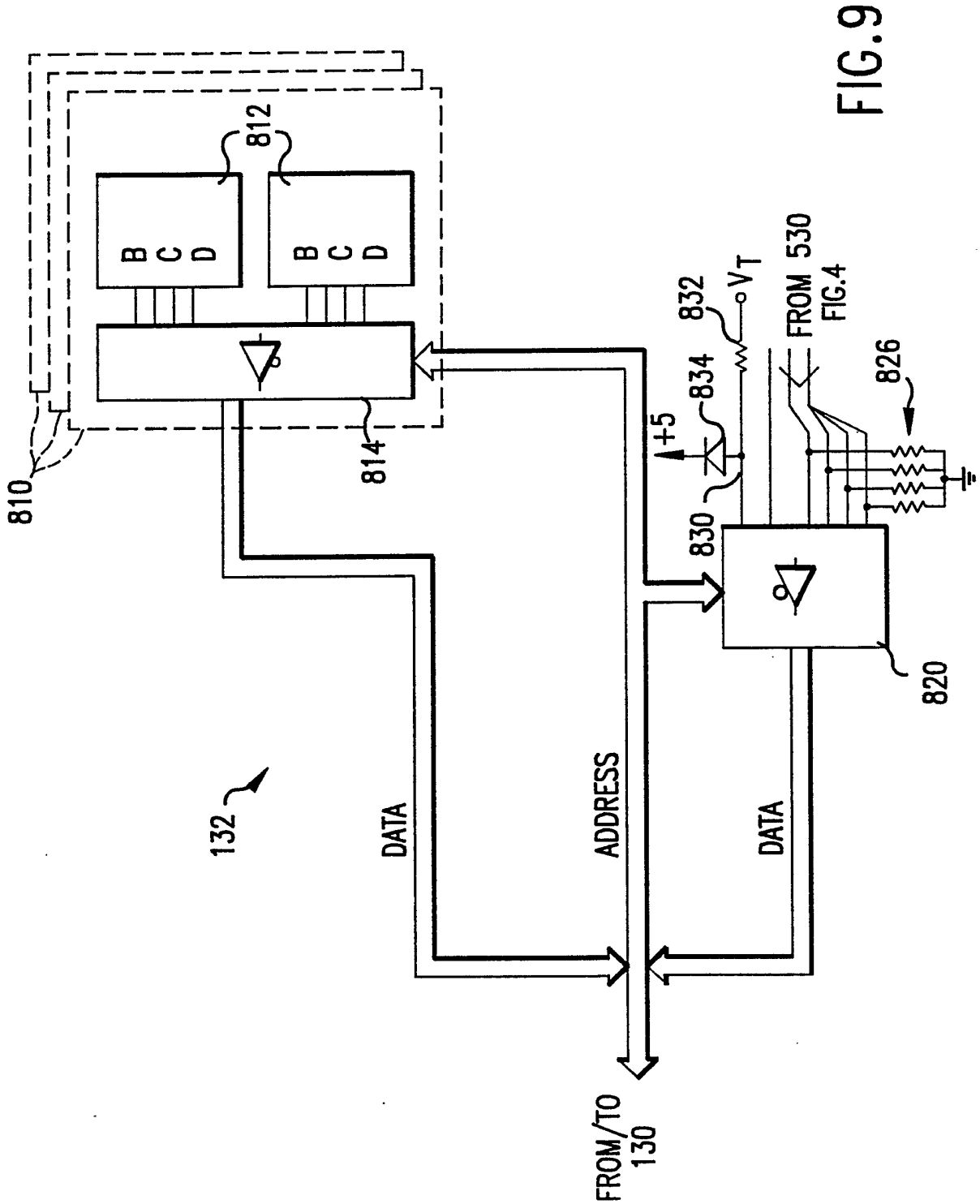

812
B C D
B C D
810
814
832
V_T
834
+5
FROM 530
FIG.4
826
830
820
132
DATA
ADDRESS
DATA
FROM/TO
130

FIG.9

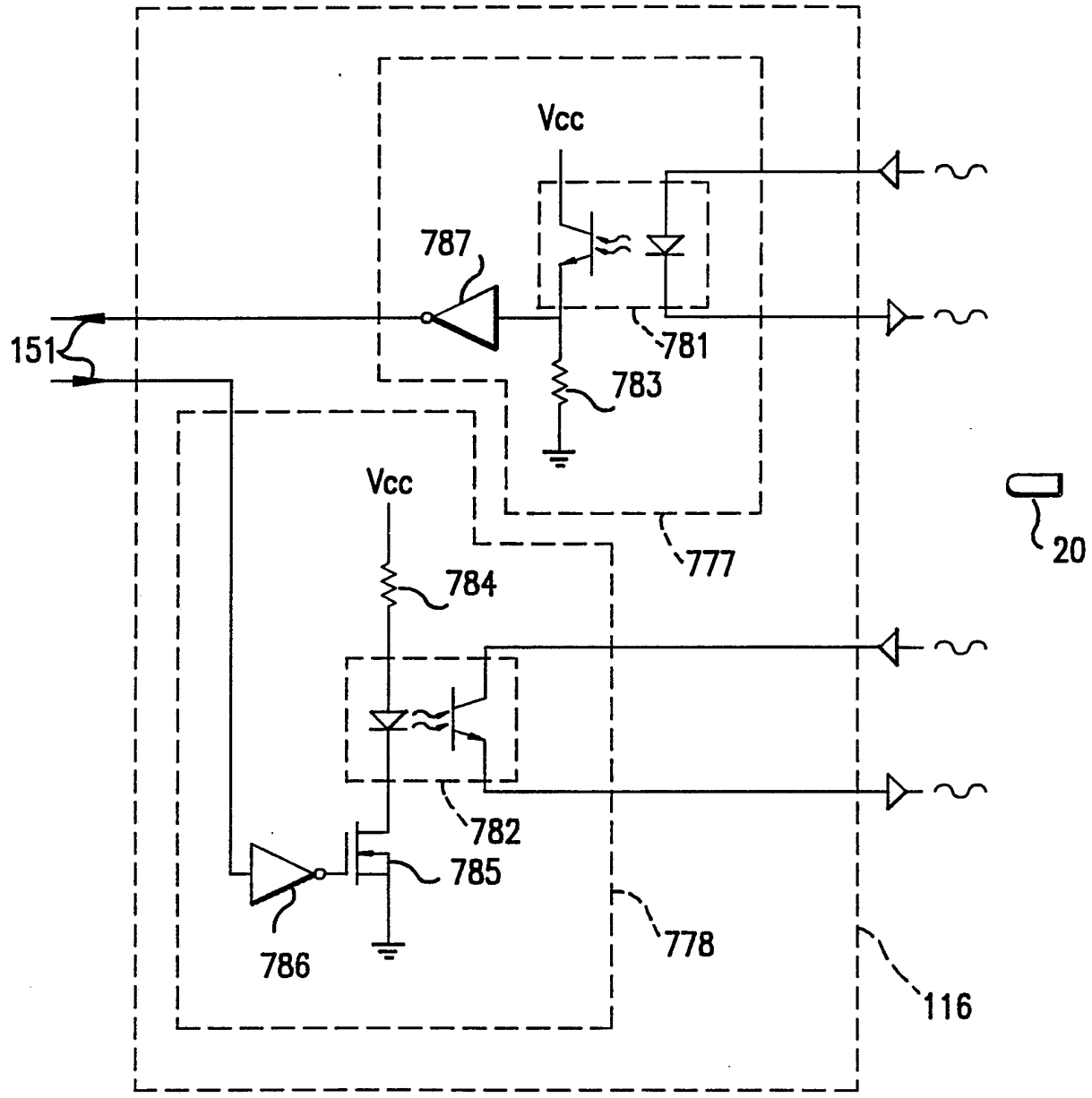


FIG.10a

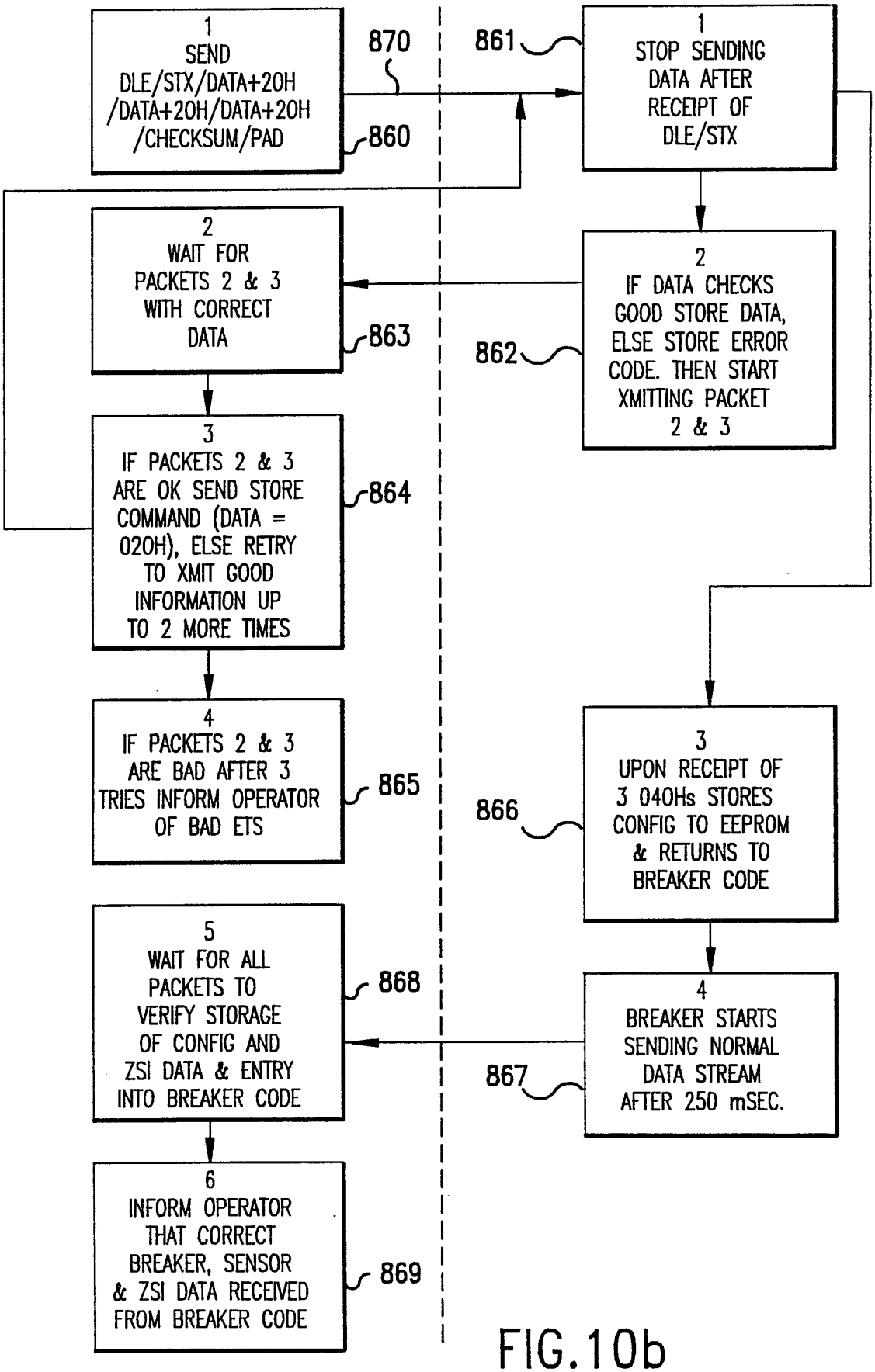

1
SEND
DLE/STX/DATA+20H
/DATA+20H/DATA+20H
/CHECKSUM/PAD
870
860
1
STOP SENDING
DATA AFTER
RECEIPT OF
DLE/STX
861
2
WAIT FOR
PACKETS 2 & 3
WITH CORRECT
DATA
863
2
IF DATA CHECKS
GOOD STORE DATA,
ELSE STORE ERROR
CODE. THEN START
XMITTING PACKET
2 & 3
862
3
IF PACKETS 2 & 3
ARE OK SEND STORE
COMMAND (DATA =
020H), ELSE RETRY
TO XMIT GOOD
INFORMATION UP
TO 2 MORE TIMES
864
4
IF PACKETS 2 & 3
ARE BAD AFTER 3
TRIES INFORM OPERATOR
OF BAD ETS
865
3
UPON RECEIPT OF
3 040Hs STORES
CONFIG TO EEPROM
& RETURNS TO
BREAKER CODE
866
5
WAIT FOR ALL
PACKETS TO
VERIFY STORAGE
OF CONFIG AND
ZSI DATA & ENTRY
INTO BREAKER CODE
868
4
BREAKER STARTS
SENDING NORMAL
DATA STREAM
AFTER 250 mSEC.
867
6
INFORM OPERATOR
THAT CORRECT
BREAKER, SENSOR
& ZSI DATA RECEIVED
FROM BREAKER CODE
869

FIG.10b

INTERNATIONAL SEARCH REPORT

International Application No.
PCT/US92/10250

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :H02H 3/00, H02J 9/00
US CL :361/64, 361/81, 361/93
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 361/68, 361/91, 361/94, 361/97

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS Text Search: Beaher#, Remote, Program?, Optical?, Relay, Signal, Data, Line#

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y,P	US, A, 5,102,664 (Haun et al) 10 November 1992, See entire document.	1,7,14
Y,P	US, A, 5,079,715 (Venkataraman et al) 07 January 1992, See abstract.	1,7,14
A,P	US, A, 5,164,875 (Haun et al) 17 November 1992, See entire document.	1-17

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search
08 FEBRUARY 1993

Date of mailing of the international search report
04 MAR 1993

Name and mailing address of the ISA/US
Commissioner of Patents and Trademarks
Box PCT
Washington, D.C. 20231
Facsimile No. NOT APPLICABLE

Authorized officer
For S. W. JACKSON
RAUTEN NGOC-HO
INTERNATIONAL DIVISION

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